Comprehensive Study of CNTFET based Positive Feedback Differential Amplifier

Thesis

Submitted to the

G.B. Pant University of Agriculture & Technology
Pantnagar-263145, Uttrakhand, INDIA

By

PREETI JOSHI
B.TECH. (Electronics & Communication Engineering)

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF

Master of Technology
in
Electronics and Communication Engineering

July, 2017

ACKNOWLEDGEMENT

During the journey towards this Master's degree, it would never be possible to come up with this thesis and all the work that went into it, without the generous assistance and support of many great people.

First and foremost, it is my immense pleasure to avail this opportunity to express my gratitude, regards and heartfelt respect to my advisor ***Dr. K.K. Sharma,*** *Assistant Professor, Department of Electronics and communication Engineering, G.B. Pant University of Agriculture and Technology for his endless and valuable guidance prior to, during and beyond the tenure of project work. His priceless advices have always lighted up my path whenever i have struck a dead end in my work. It has been a rewarding experience working under his supervision as he has always delivered the correct proportion of appreciation and criticism to help me excel in my field of research.*

I would like to express my gratitude and respect to my committee members, ***Dr. Abhishek Tomar, Dr. Paras,*** *Assistant Professor,* ***Department*** *of Electronics and communication Engineering,* ***Dr. Abhishek Yadav,*** *Assistant Professor, Department of Electronics and Electrical Engineering for their support, feedback and guidance throughout my M.Tech. course duration.*

I am thankful to ***Dr. Devendra Kumar****, Dean, College of Post Graduate Studies and* ***Dr. H.C. Sharma****, Dean, College of Technology, G.B. Pant University of Agriculture and Technology, Pantnagar for providing necessary facilities to carry out the study.*

I would also like to thanks all the faculty and staff of ECE department, G.B.P.U.A.T. Pantnagar for their support and help during the two years of my student life in the department.

I am also very thankful to all my friends and seniors who always encouraged me in the successful completion of my thesis work.

I thank the gracious Lord for all his numerous blessings bestowed upon me in various ways. At this juncture of time my heart is full and I feel short of words at my command to express my respect to my beloved parents whose invaluable love and support have brought me to this position.

Preeti Joshi

(Preeti Joshi)
Authoress

Pantnagar
July, 2017

CERTIFICATE I

This is to certify that thesis entitled **"Comprehensive Study of CNTFET based Positive Feedback Differential Amplifier"** submitted in partial fulfilment of the requirements for the degree of **Master of Technology** with major in **Electronics and Communication Engineering** of the College of Post-Graduate Studies, G. B. Pant University of Agriculture and Technology, Pantnagar, is a record of bona fide research carried out by **Ms. Preeti Joshi**, Id. No. **49400** under my supervision and no part of thesis has been submitted for any other degree or diploma.

The assistance and help received during the course of this investigation and source of literature have been duly acknowledged.

Pantnagar
July, 2017

(K.K. Sharma)
Chairman
Advisory Committee

CERTIFICATE II

We, the undersigned, members of the Advisory Committee of **Ms. Preeti Joshi**, Id. No. **49400**, a candidate for the degree of Master of Technology with major in Electronics and Communication Engineering, agree that the thesis entitled "**Comprehensive Study of CNTFET based Positive Feedback Differential Amplifier**" may be submitted in partial fulfilment of the requirements for the degree.

(K.K. Sharma)
Chairman
Advisory Committee

(Abhishek Tomar)
Member

(Abhishek Yadav)
Member

(Paras)
Member

CONTENTS

S. No.	CHAPTERS	PAGE No.
1	Introduction	
2	Review of Literature	
3	Materials and Methods	
4	Results and Discussion	
5	Summary and Conclusion	
	Literature Cited	
	Appendix	
	Vita	
	Abstract	

LIST OF TABLES

TABLES	TITLE	PAGE NO
3.1	Scope of the CNTFET Model	
3.2	Features of different Technology nodes	
3.3	Values of different parameters for 32nm Technology node	
4.1	CMOS Differential Amplifiers at 32nm	
4.2	CNTFET Differential Amplifiers at 32nm	

LIST OF FIGURES

FIGURES	TITLE	PAGE NO
1.1	Block Diagram of internal Circuit of Operational Amplifier	
3.1	Classification of Silicon IC Technology	
3.2	Structure of MOSFET	
3.3	PMOS n-well Structure	
3.4	MOS Symbols	
3.5	Immunity to Noise signal	
3.6	(a) Corruption of a signal due to coupling	
	(b) Reduction of coupling by differential operation	
3.7	Current Mirror Load	
3.8	Source Degenerated Resistive Feedback	
3.9	Split Signal Differential Amplifier	
3.10	Resistive Common mode Feedback Differential Amplifier	
3.11	Resistive Feedback with cross coupling	
3.12	Cascoded Differential Amplifier	
3.13	Positive Feedback Differential Amplifier	
3.14	Resistive Load Differential Amplifier	
3.15	Variation of Drain current with Input voltage	
3.16	Effect of Common noise on output signal	
3.17	Variation of Output voltage with Common mode voltage	
3.18	Charging and discharging of Output Capacitance	
3.19	Block diagram of Positive Feedback Circuit	
3.20	Positive Feedback cross coupled differential Amplifier	

3.21 Small signal model of Positive Feedback Differential Amplifier

3.22 Single walled and Multi walled Carbon Nanotube

3.23 Internal Structure of Carbon Nanotube

4.1 Transfer Characteristics of CMOS differential Amplifier with Active Load

4.2 Frequency response curve of CMOS differential Amplifier with Active Load

4.3 Phase Curve of CMOS differential amplifier with Active Load

4.4 Transfer Curve of CMOS Source Degeneration Differential Amplifier

4.5 Frequency response of CMOS Source Degeneration Differential Amplifier

4.6 Phase Curve of CMOS Source Degeneration Differential Amplifier

4.7 Transfer Curve of CMOS Multiple Signal Differential Amplifier

4.8 Frequency response of CMOS Multiple Signal Differential Amplifier

4.9 Phase Curve of CMOS Multiple Signal Differential Amplifier

4.10 Transfer Curve of CMOS Resistive Common mode differential Amplifier

4.11 Frequency response curve of CMOS Resistive Common mode Differential Amplifier.

4.12 Phase Curve of CMOS Resistive Common mode Differential Amplifier

4.13 Transfer Curve of CMOS Resistive cross coupled common mode feedback differential amplifier

4.14 Frequency response Curve of CMOS Resistive cross coupled common mode feedback differential amplifier

4.15 Phase Curve of CMOS Resistive cross coupled common mode feedback differential amplifier

4.16 Transfer Curve of CMOS Positive Feedback Differential Amplifier

4.17 Frequency response curve of CMOS Positive feedback differential amplifier

4.18 Phase Curve of CMOS Positive Feedback Differential Amplifier

4.19 Transfer Curve of CMOS Cascoded Differential Amplifier

4.20 Frequency response curve of CMOS Cascoded Differential Amplifier

4.21 Phase Curve of CMOS Cascoded Differential Amplifier

4.22 Transfer curve of CNT Differential Amplifier with Active Load

4.23 Frequency response curve of CNT Differential Amplifier with Active Load

4.24 Phase curve of CNT Differential Amplifier with Active Load

4.25 Transfer curve of CNT Source Degeneration Differential Amplifier

4.26 Frequency response curve of CNT Source Degeneration Differential Amplifier

4.27 Phase curve of CNT Source Degeneration Differential Amplifier

4.28 Transfer curve of CNT Multiple Signal Differential Amplifier

4.29 Frequency response curve of CNT Multiple Signal Differential Amplifier

4.30 Phase curve of CNT Multiple Signal Differential Amplifier

4.31 Transfer curve of CNT Resistive Commmon mode Differential Amplifier

4.32 Frequency response curve of CNT Resistive Commmon mode Differential Amplifier

4.33 Phase curve of CNT Resistive Commmon mode Differential Amplifier

4.34 Transfer curve of CNTFET Resistive Cross coupled common mode differential Amplifier

4.35 Frequency response curve of CNTFET Resistive Cross coupled common mode differential Amplifier

4.36 Phase curve CNTFET Resistive Cross coupled common mode differential Amplifier

4.37 Transfer curve of CNTFET Positive Feedback Differential Amplifier

4.38 Frequency response curve of CNTFET Positive Feedback Differential Amplifier

4.39 Phase curve of CNTFET Positive Feedback Differential Amplifier

4.40 Phase curve of CNTFET Positive Feedback Differential Amplifier

4.41 Frequency response curve of CNTFET Cascoded Differential Amplifier

4.42 Phase curve of CNTFET Cascoded Differential Amplifier

LIST OF ABBREVIATIONS

FET	Field Effect Transistor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Field Effect Transistor
IC	Integrated Circuit
CNT	Carbon Nanotube
MWNT	Multi Walled Nanotube
SWNT	Single Walled Nanotube
CNTFET	Carbon Nanotube Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N type MOSFET
PMOS	P type MOSFET
dB	Decibels
DC	Direct Current
CMRR	Common Mode Rejection Ratio
GaAs	Gallium Arsanide

LIST OF SYMBOLS

λ	Channel Modulation
w/l	Size ratio of CMOS
μ	Micro
g_m	Transconductance
V_{gs}	Gate to Source Voltage
V_{ds}	Drain to Source Voltage
I_{SS}	Current Source
C_L	Load Capacitance
C_{OX}	Oxide Capacitance
V_{dd}	Supply Voltage
I_d	Drain Current
µ	Mobility
R_0	Output Resistance
V_t	Threshold Voltage
A_{od}	Differential Gain
A_{ocm}	Common mode Gain
R_f	Feedback Resistance
R_s	Source Resistance

Introduction

Chapter 1 INTRODUCTION

Though Digital and Mixed signal processing have moved to the Integrated Circuit domain, but analog circuits have proved fundamentally necessary in many of today's complex high performance systems. A common digital interface, the differential line needs an analog circuit to function well. The receiver must filter out common mode interference by computing the analog difference between the two lines. Most digital interfaces are designed as analog, only a few legacy interfaces (which have poor performance) use entirely digital circuits. Many radio signals are simply too high frequency to work with existing digital circuits. Radio modulators, demodulators, mixers, transmitters, and receivers are still analog. Some signals are even too high frequency for transistor circuits of any kind to amplify efficiently, such as microwave signals, which are still transmitted using vacuum tubes. Many devices, such as monitors, require analog control. Even LCD monitors require analog circuits, although they need not be as sophisticated as CRT analog circuits. Audio equipment requires analog circuits. Speakers must be driven by analog signals, microphones produce analog signals. Signal of a microphone must be conditioned before conversion to digital, this usually entails sophisticated analog circuits such as preamplifiers, compressors, and filters.

Applications such as high definition television (HDTV), compact disc players, CD ROM, and modems, as well as special systems such as medical imaging, speech processing, and radar employ data conversion systems for interfacing. In most of the data conversion systems, such as switched capacitor circuits sigma-delta converters, pipeline A/D converters, algorithmic A/D converters and sample-and-hold amplifiers, amplifiers form the basic building block.

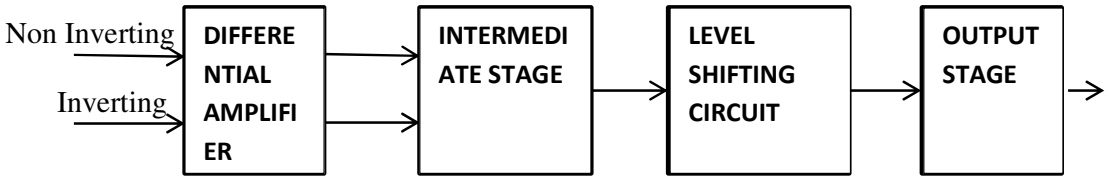


Figure 1.1 Block Diagram of Internal Circuit of Operational Amplifier

Differential amplifier is a device which forms an essential part of most of the analog circuits. It acts as an input stage of operational amplifier circuit which amplifies the difference between signals applied at both the inverting and non -inverting inputs regardless of common mode input. Initially differential amplifier was made with the help of vacuum tubes subsequently with the evaluation of technology we came cross BJT differential amplifier. However, it was the adventure of IC that made differential amplifier so important in both bipolar and MOSFET. There are basically two reasons for such suitability of differential amplifier for IC fabrication. Firstly, the performance of differential amplifier depend on matching criteria between both side of the circuit and Integrated circuit are able to provide matched devices which takes into consideration various environmental changes. Secondly, differential amplifier employs more components than their single ended counterparts, here again availability of large number of transistors with integrated circuit technology proved advantageous.

But, why differential over single ended circuit? The answer to this lies in the facts that when we use differential signal then the coupled noise signal get distributed equally between both differential signal of opposite phase and at the output we get only differential amplified signal with no interference signal. The other reason is that the differential configuration makes biasing much easier and helps to pair amplifier stages thus avoiding the need of bypass or coupling capacitors like those used in discrete circuits which make fabrication of large circuits economically impossible.

A large number of devices use differential amplifiers as an internal circuit. The output of an ideal differential amplifier can be given as:

$$V_{out} = A_d(V_{in1} - V_{in2}) \quad (1.1)$$

Where, V_{in1} and V_{in2} are input voltages and A_d is the differential gain. If V_{in1} and V_{in2} are equal, then output will not be zero as in practice gain is not equal for two inputs. A more practical expression for the differential amplifier output includes an additional term

$$V_{out} = A_d(V_{in1} - V_{in2}) + A_c\left(\frac{V_{in1}-V_{in2}}{2}\right) \quad (1.2)$$

A_c is called the common mode gain of the amplifier.

Today analog circuits design encounter many limitations these are mainly because of continuous demand for integrated chip process technologies, advanced electronic systems and complex circuit integration. With this comes the increasing demand for high speed, low power, low noise and high gain devices. This has given rise to advanced CMOS technology which deals at sub-micron regime that is technology node below 90nm. At this scale, process variation becomes critical issue for circuit design. Downsizing of device at 32 nm reduces the dopant count to below 30 which leads to some major challenges like mismatches. These process variations include change in oxide thickness, temperature, and dopant fluctuations which have an impact on the performance of circuit. These variations can be minimized with the use of device known as Carbon Nanotubes. Carbon nanotubes are more compatible to work with short length devices therefore can be seen as a substitute for CMOS.

CNTFET is one of the most promising technologies developed to function in the scale of 1nm to 100nm. CNT are made up of graphite sheet whose dimensions are given by its chirality. Carbon nanotubes offer many advantages over CMOS like with change in diameter of tube one can control threshold voltage. It provides high mobility, better electrostatics, flexible pitch and number of nanotube. CNT possesses characteristics like extraordinary strength, ballistic transport and support easy integration of high dielectric constant material. Diameter of the CNTFET can be increased in order to have large bandwidth smaller effective pitch which strongly affects the outer fringe and Cgc capacitances. It is primarily due to enhanced screening between adjacent channels. The power consumption of the amplifier increases due to smaller band gap as CNTs become more conducting thereby, enhancing the current drive.

1.1 MOTIVATION

The Op Amp circuit consist of three stages in which first one consist of differential amplifier. Differential amplifier is a basic building block of Op Amp, it supresses the noise present at the input signal and amplifies only the difference between two signals thus providing high gain input for op amp. In CMOS, due to miniaturization of device size, mismatches, variations and leakage current starts dominating. CNTFET can be seen as the solution for this as it has better control over short channel effects. By varying parameters like

Diameter, pitch one can obtain desirable current drive. Therefore one of the gain enhancement topology i.e. positive feedback differential amplifiers has been designed using CNTFET at 32nm. Positive feedback Differential amplifier which consists of cross coupled differential pair generates negative trans conductance which get cancelled by the trans conductance produced by pmos load and nmos pair thus increasing the overall gain of the differential amplifier. In case of classical differential amplifier output swing is limited by threshold voltage but with feedback output swing is limited by voltage which is much less than threshold, therefore greater output swing is attained. Beside this other parameters which determine the performance of diff amp include bandwidth, slew rate, DC gain and power dissipation. Our motivation is to design high gain, large bandwidth differential amplifier for low power dissipation.

1.2 Objective of the thesis

As Differential amplifier forms the initial stage of operational amplifier so its designing plays very crucial role for proper working of the circuit. It is desirable that a differential amplifier should have high gain so that large signal at the input of intermediate stage. Moreover the signal should be noise free to have minimum distortion that means high Common Mode Rejection Ratio is required. Carbon nanotube has been used to replace CMOS differential amplifier as CNT provide high gain and bandwidth as it possess low junction capacitance and high trans conductance. By selecting optimum number of tubes biasing voltage and current could be set.

The main objective of the proposed work is:

i) To design and simulate the differential amplifier for high gain.
ii) To improve the CMRR of Differential amplifier
iii) To increase the Unity Gain Bandwidth
iv) To reduce the power dissipation

The performance of the proposed differential amplifier is evaluated using the following CMRR formula:

$$CMRR = A_d/A_C$$

where A_d is defined as differential mode gain which can be obtained by applying equal and opposite signal at both the inputs whereas A_C can be calculated by applying

same value at the input. Therefore CMRR that is Common Mode Rejection Ratio can be given by ratio of differential gain to common mode gain. Output Voltage can be given by:

$$Vo = A_d V_d + A_c V_c$$

Where, A_d is differential Gain and A_C is Common mode Gain.

1.3 Research Problem

This work will analyse the various parameters like gain, bandwidth, power dissipation of cmos positive feedback differential amplifier. Positive feedback enhances the differential gain of the circuit. Selection of any differential amplifier is made on the basis of Gain and CMRR which is considered as its figure of merit. While working at nanoscale or at technology node at 45nm, 32nm various fluctuations and mistaches become dominant due to process variation which degrades performance of the circuit. In order to lessen the effect of these mismatches while improving performance of the circuits CNTFET has been implemented replacing CMOS. Carbon nanotubes incorporates ballistic transport, high mobility, provide better current drive for the same circuit.

HSPICE is an analog circuit simulator used to perform transient, frequency domain and steady state analysis. It allows hierarchical node naming, circuit optimization, input, output, and behavioural algebrics for parameterized cells and interactive waveform viewing with Cosmos cope. Using HSPICE we can compute: Gain, Unity Gain Bandwidth, Power dissipation and CMRR.

Review of Literature

Sackinger *et al* (1987) has extended the concept of operational amplifier using two differential inputs. Also a simple differential difference amplifier circuit has been presented including all its non idealities, operating parameters and voltages. Some non idealities which restricts the performance of the circuit has been recognised and analysed mathematically. Several applications which employs less number of components than operational amplifiers has been discussed. Difference which is pointed out between ordinary and DDA is that the ordinary amplifiers have wired feedback and its closed loop gain can be moved by gain factor of transconductance elements, whereas in DDA gain factor is fixed thus saving requirement of external component.

Matthews (1997) has devised a new topology for differential CMOS buffer amplifier with well controlled voltage gain. The new buffer amplifier consist of a transistor in feedback loop which reduces the output resistance and hence effect of trans conductances on gain decreases. Besides this effects of small signal sensitivities also been tested and results shows new design new buffer offers reduced sensitivity to variations in both channel-length modulation and carrier mobility. The circuit was simulated using models for an n-well CMOS process. Also the factors affecting the frequency response of the circuit has been discussed.

Takenaka *et al.* (2000) have proposed class AB differential amplifier which has reduced the power dissipation of Wang OTA from 244µW to 46µW.A new tail current source circuit has been put forward that uses voltage mode circuit in place of current mode which in turn reduces chip area .Simulations are done using HSPICE with 2µm process technology. Result when compared by Wang's amplifier shows that the proposed design has greater linear output range. Moreover the cutoff frequency came out to be much lower than that of Wang's design. Though some complexity of circuit is increased but is overpowered by its low power driving capabilities.

Zeljko *et al.* (2004) has discussed the small signal analysis of single ended CMOS differential amplifier with active load. They have taken into consideration the body effects and analytical calculations have been performed. Simulations are done at

0.25 micron feature size using SPICE BSIM3 model to find values of various parameters required for analysis. Analytical and spice analysis result is different in case of simple circuit whereas these two result are same when condering body effect in performing analytical analysis. This is found because spice works by including body effect.

Lin *et al.* (2005) has presented a new design of two stage CMOS differential amplifier which provide high bandwidth and greater dynamic output range. The first stage of the circuit is basically a telescopic configuration that helps to provide enough gain for entire circuit and consumes less power. The output of first stage works as common mode feedback for transistors which are used for regulating tail current. The second stage is simply a common source architecture that is used to get high swing at the output of the amplifier. Simulations has been performed using CSMC 0.6μm CMOS process technology for 5V power supply. On evaluation the output swing of the circuit comes out to be ±4.75V, gain of about 86.8db, bandwidth is 966MHz and dynamic output range of 84.4db.

Giustolisi *et al.* (2007) has presented a pseudo differential amplifier in class AB working in CMOS technology .The circuit is characterised by minimum supply voltage of $V_T + 2V_{DS,SAT}$, wide range of input voltage, more linearity which makes it suitable even for filter application as a transconductor. The common mode feedback circuit has been included to enhance its performance. Circuit fabrication has been carried out using 0.35μm process under supply of 2V.Simulation is done in Cadence spectre and compared the proposed design specifications with that of traditional one. The proposed circuit has shown big improvement in PSRR which is 73db, maximum current drive of 500 μA and good linearity.

Wu *et al.* (2008) has designed a differential amplifier with high gain and high linearity. The design is based on negative impedance compensation technique which offer more precision, low sensitivity with wide input signal range. At a particular frequency gain accuracy and linearity can be improved by using a capacitor in series with a correction resistor. The concept behind is basically to compensate differential amplifier by local feedback using floating negative impedance circuit which is a cross coupled transistor circuit connected between two input terminals. Results shows an improvement of about 27 percent.

Wangtaphan *et al.* (2009) has employed a CMOS inverter based transimpedance amplifier with noise cancelling circuitry. The circuit consist of a CMOS inverter and current mirror. The performance has been evaluated using HSPICE with 0.13μm CMOS technology under power supply of 1.2V.The bias point is designed as such in order to achieve low power and high bandwidth.The output impedance of the circuit comes out to be 5.2kΩ.The noise figure is around 2.32Ghz.Moreover the input impedance is designed to match with the source impedance which helps in achieving maximum power transfer and minimum reflection.

Raikos *et al.* (2009) has analysed a low voltage based differential amplifier using bulk driven PMOS transistors. Moreover a positive feedback has been used to boost up input transconductance and noise performance. Besides this, a 5^{th} order Chebyshev active RC filter has been made with 500 Khz cut-off frequency and 1dB ripple. Results are obtained by using cadence tool under 0.35μm process technology of supply 3.3V.The gain of the proposed amplifier in worst case comes out to be 45db for the said frequency.

Xiaojun *et al.* (2010) has devised a new technique for higher frequencies differential power amplifiers which improvises the stability and gain of the circuit. In order to show the impact, 60 GHz differential power amplifier has been designed using 90nm CMOS process technology. To neutralize the parasitic effect, capacitors with cross coupling are introduced. For analysis S parameters has been calculated and performed using Anritsu VNA, whereas calibrations has been carried out using methodology of LRRM for frequency range of 1 to 100 GHz. Results demonstrated that this circuit has low power consumption of 52mW, gain of 10 db and bandwidth of 6.3GHz, thus making it suitable for 60GHz transceiver systems.

Enche *et al.* (2010) has demonstrated a CMOS folded cascoded differential amplifier for higher frequency range. A detailed theoretical study is done and various parameters that influence the design are analysed .The fully differential amplifier need a common mode feedback circuit in order to predict the common level of outputs and tune the bias current accordingly. The proposed design has been implemented in CADENCE tool under CMOS 0.18μm technology for 3.3V supply voltage. Simulations has shown circuit gain of 63.12db, phase margin is 56.9.

Suadet *et al.* (2010) has proposed a CMOS inverter based class-Ab pseudo differential amplifier in which complementary common mode feedback comprises of current mode detector and transimpedance amplifiers. Simulations has been performed in spectre using 0.18um CMOS process with 1V supply voltage. In this design bias currents of all transistors are selected in order to optimize power dissipation and gain. Results has shown DC gain of 36dB,unity gain frequency of 800MHz and -3dB frequency can be attained at 8.5MHz.

Pude *et al.* (2010) has devised positive feedback as a remedy to increase gain at scaled down technologies. A generalised study has been carried out including all non idealities like limited input impedance, non-zero output impedance etc. The design has been fabricated using TSMC's 65nm process technology and the circuit is evaluated with HP4156A Precision parameter analyser. Monte Carlo Simulation has been done and compared with that of Silicon for device mismatch and process variations. Results depicted hysteresis in the Positive Feedback Amplifier which lead to false switching. Though there is an increase in standard deviation but increase in gain is high enough for its compensation and thus provide worst case gain enhancement.

Fahad Ali *et al.* (2010) has put forward complete optimal design of an inverting amplifier in CMOS,CNTFET and mixed technologies. The performance evaluation of amplifier with variations in parameters like number of nanotubes, pitch, and operating voltage has been carried out for CNTFET. Besides that it has also investigated the challenges expected to occur while working at Nano scale. From the analysis and various plots it has been concluded that hybridization can be useful for applications which require large bandwidth and output driving capability if used NMOS-PCNTFET device whereas for achieving better transient performances PMOS-NCNTFET device can be employed. Another important conclusion is that diameter of CNTFET plays crucial role in determining performance of circuit as almost all properties are dependent on it.

Ab Rahim *et al.* (2011) has presented single stage fully differential cascaded amplifier with gain boosting technique. It comprises of two circuits a 12 bits pipelined analog to digital converter followed by gain booster. Amplifier is implemented in 0.13µm CMOS process technology. Simulations has shown that a DC gain of 95db, bandwidth of 414Mhz and phase margin of 82 degrees can be obtained at power supply

of 3V and load capacitance of 2pf.Settling time for the present circuit comes up to be 6.17ns with power dissipation of 11MW.

Simonetti *et al.* (2011) has introduced a compensation technique for Switched Capacitors Common Mode Feedback loop for a differential difference amplifier which increases its loop gain and bandwidth. This technique incorporates positive feedback which introduces a zero thus enhancing the phase margin of the common mode feedback loop. Simulations has been carried out in 0.13um CMOS technology using Cadence spectre with supply of 1.2V.Results have shown that the proposed technique is successful in obtaining better common mode rejection over wider frequency range without affecting main differential path.

Bharatha Kumar *et al.* (2011) has presented a wideband amplifier with high performance. The power is very low about 6.8MW under supply voltage of 1.8V. The cross coupled cascade topology has been incorporated in order to improve bandwidth and gain. The proposed design is fabricated using 0.18μm SiGe BiCMOS process. Measurement of the amplifier has been done using Vector Network Analyzer. Results shows that the design is less prone to various process variations with small signal gain of 9.3db for 3db bandwidth of 14.3GHZ. The noise figure plot suggests a flat noise value till 10.1 GHZ then increases gradually for drop in gain with rise in frequency.

Chouard *et al.* (2011) have performed Stress experiments on analog size devices in inversion and accumulation mode, including relaxing stress phenomena. Based on these data, a general concept to suppress device aging impact on differential amplifier circuits in advanced CMOS technologies is presented and proven experimentally. It is shown that the proposed method also enables to compensate for process variation induced mismatch. This study was proven by experiments using PBTI degradation at an nMOS input pair. Thus it provides analog circuit designers the opportunity to reduce matching related area requirements.

Vladimir *et al.* (2012) has compared self biased complementary single ended differential amplifier with fully differential amplifier. Both the amplifiers uses negative feedback loop which stabalizes the biasing voltage against process and temperature variation at the operating point while operating deep within linear region. Small signal analysis of both circuit is performed and expression of gain has been derived. Simulation is done using 40nm low power CMOS technology. Results have shown

fully differential amplifier provides better gain, bandwidth, threshold and drain current which makes it preferable for use in nanometer regime.

Tran *et al.* (2012) have designed a differential amplifier with positive feedback loop which uses horizontal cross coupled transistors between input and output and this produces negative trans conductance. At the output this trans conductance get cancel out as a result a very high differential gain get generated. Besides that in order to tune the circuit against process temperature variation and vary the gain an adjustable voltage bias has been provided. The simulation is performed using LT spice in 90nm CMOS process technology. The advantage of the design is larger output voltage swing, larger gain and better unity gain bandwidth.

Kawamura *et al.* (2012) has designed a differential amplifier for smartphone sensing at low voltage driven by audio interface with no external supply. The sense circuit of amplifier comprises of rectifier, voltage divider, earphone and microphone terminals. The proposed pseudo differential amplifier is inverter based and used as signal processing section of smartphone. Simulations has been performed using 0.18μm standard CMOS technology at supply voltage of 1V. The measured values of specifications are like 51.4db of maximum gain, CMRR of around 45.1db and offset input temperature is 1.5μV/ ℃.

Wilson *et al.* (2013) has proposed a current starved inverter based differential amplifier designed in a commercial 0.18um process. It consist of two pairs of cmos inverter at the input which increases the gain of the circuit and employs active load with four additional inverters, inner pair of inverters provide negative resistance and the outer pair provide positive resistance thus providing overall high output impedance. The simulations are performed for three different supply voltages of 0.7V, 0.9V and 1.1V operating at various levels of sub threshold region. Result has shown design achieves 46dB DC gain and a 464 kHz unity gain frequency with a power consumption of only 145.32nW at 700mV power supply voltage. Also this circuit is simple to design and provide better current control.

Hsu *et al.* (2014) proposed a 0.6V-1.2V fully-differential amplifier with pulse-controlled common-mode feedback circuit realized in low power/leakage 65nm CMOS

technology. The pulse controlled common-mode feedback circuit results in a fully differential amplifier with large output swing but less area cost than conventional common-mode feedback circuits. When the supply is varied from 0.6V to 1.2V, the measured frequency response deviations are small and the measured output noise spectrum density only changes from 21.5nV/pHz to 30.3nV/pHz showing the flexible supply operation of the differential amplifier with the PC CMFB.

Jagadish *et al.* (2014) have presented a low voltage and low power inverter based differential amplifier. The circuit input stage is fully differential while output consist of class C inverter which enhances the gain. Transistors are sized to operate in sub threshold region under DC operating conditions. Simulation is done using Cadence tool with UMC 90nm library cell. For a load capacitance of 100fF, the amplifier delivers DC gain of 81dB and unity gain bandwidth of 33.88MHz at 41◦ phase margin. For a dual power supply voltage of 350mV, the quiescent current and power consumption are 2.37μA and 1.66μW respectively. The amplifier achieves a figure of merit of 2117.

Vikhe (2015) has designed single stage differential amplifier of 32nm gate length and done analysis in three different technologies namely MOSFET, CNTFET, FINFET. The simulation is performed in hspice and various parameters like slew rate, CMRR, frequency response, gain and power consumption. Observations have shown differential amplifier design using MOSFET has unity gain bandwidth 1100MHz which is good compared to the designs using CNFET and FinFET whereas FINFET offers open loop Gain 18.5 dB, Slew Rate 19.2E+06 V/μsec, CMRR 11.34 dB which is best for given gate length.

Amina *et al.* (2015) have taken an analytical approach to accurately determine common-mode rejection ratio (CMRR) considering the effects of various non-idealities such as the presence of channel length modulation, body effect, finite resistance of the current source, mismatches in transconductances and drain resistances between the two driver MOSFETS of a common source CMOS differential amplifier. This analysis brings to light the hitherto unforeseen dire impacts of these non-idealities put together on CMRR, and hence strongly suggests that these effects should not be, in any ways, ignored from theoretical calculations for CMRR. The simulation have been carried out considering standard 0.5um process. In both cases, the results obtained considering all

non-idealities stated here are compared with those that are obtained from equations based on conventional approaches, where the effects of some of the non-idealities have been ignored. It is clear that CMRR decays, as expected, exponentially with the increased gm mismatches.

Cai *et al.* (2015) have proposed simple slew-rate enhancement (SRE) technique for fully-differential amplifier. The proposed SRE feedback is only valid during slewing, while completely blocked at DC for avoiding multiple operating points problem. The advantage of the proposed SRE method is that both positive and negative slew-rate of fully-differential amplifier can be equally improved with a very small static power overhead. Two fully differential two-stage amplifiers are designed in the IBM 130nm process The simulation result shows that the average slew-rate for a fully-differential folded-cascode amplifier can be enhanced by factor of 2.6 and the 1% settling time is reduced by 30% by comparing with the one without SRE. With such improvement, each stage of the amplifier can achieve equal slew-rate for maximizing overall slew-rate of the amplifier.

Bender *et al.* (2015) this paper presents a simple and low-cost test methodology applied to fully differential amplifiers (FDAs). This kind of amplifier needs a common mode feedback (CMFB) circuit to keep the output common mode tightly controlled. In this work we propose the reuse of the CMFB circuit of FDAs as an embedded checker to ease the test of the whole amplifier, increasing the observability of faults occurring either in the amplifier or in the CMFB block. Catastrophic faults are injected into these two circuits by means of SPICE simulations, considering a 0.18μm FDA as case study. Transient and DC (Direct Current) tests are performed and the fault coverage is evaluated. Simulation results point to high fault coverage, while only the common mode feedback signal needs to be monitored. This way, a low-cost and low area overhead test methodology is achieved with affordable test time. The total fault coverage obtained in the fault injection simulation campaigns is 97.62% by considering a complete catastrophic fault model in the amplifier transistors.

Materials and Methods

CMOS technology basic concept was developed around in 1963 by Frank Wanlass.The idea or the concept was that a circuit could be made with different complementary MOS devices, like NMOS (n channel) and PMOS (p channel) transistors.

CMOS technologies steadily captured the market due to its advantages like low power dissipation that too during switching operations and requirement of very few devices over its bipolar counterpart or GaAs. Furthermore very soon it was discovered that dimensions of MOS devices could be scaled down easily which reduced the fabrication cost of CMOS. The device scaling in future became principal force for domination of CMOS technology in analog market. The intrinsic speed of MOS device has gone up by more than three order over past 30 years. Figure 3.1 gives the distribution of Silicon IC Technology

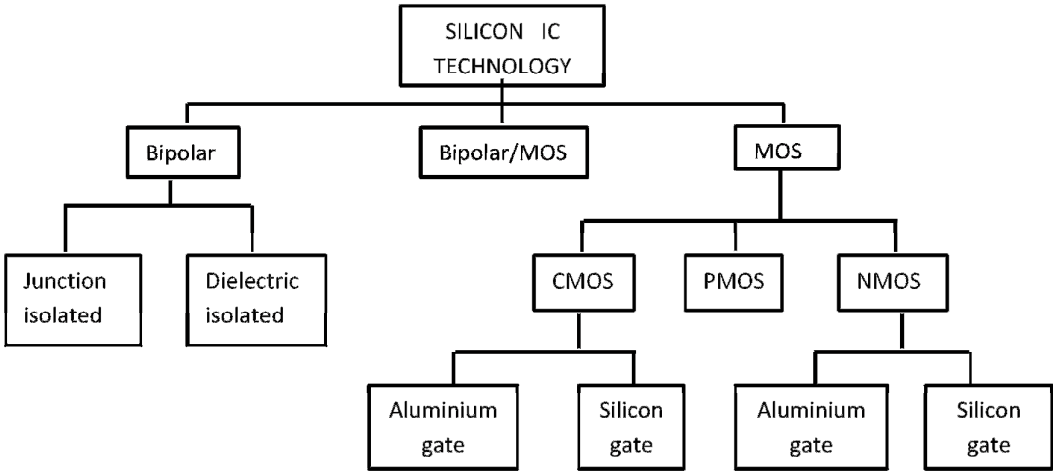


Figure 3.1: Classification of Silicon IC Technology

3.1 Structure of a MOS device: The device consist of two heavily doped n regions which form source and drain terminals, a heavily doped polysilicon operating as gate, a thin layer of silicon dioxide insulating gate from substrate as shown in Figure 3.2.

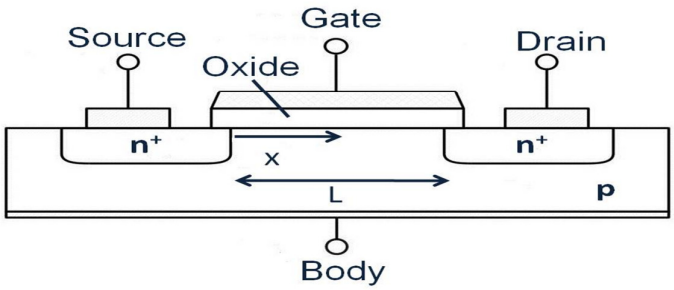


Figure 3.2 Structure of MOSFET

The dimension of gate along moving from source to drain path is called length L and perpendicular to the length is known as width. Since during fabrication the S/D junction "side diffuse", the actual distance between source and drain is little less than L. This length is known as effective length thus gate oxide thickness and effective length plays an important role in the performance of MOS circuits.

In complementary MOS technology both NMOS and PMOS are present on same wafer or substrate. For this, one of the device can be placed in a "local substrate" usually known as "well". In most of CMOS processes, the PMOS is fabricated in *n*-well. This n-well should be connected such that S/D junction of PMOS remain in reverse bias all the time as shown in figure 3.3

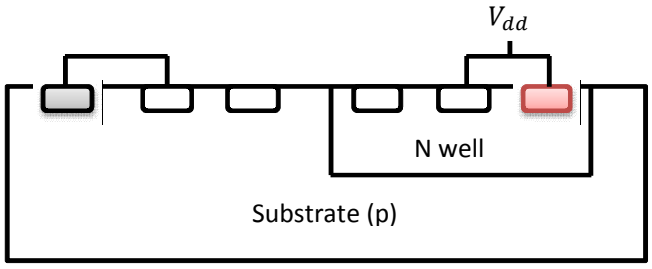


Figure.3.3 PMOS n-well Structure

Amplification is an essential function in most analog circuits. It is required as the signal provided by transducers is too weak for reliable processing and is much easier if signal magnitude become larger.

3.2 MOS Symbols: Figure 3.4 consist of circuit symbols which represents PMOS and NMOS transistors. These symbols consist of four terminals namely source, drain, gate and substrate. The source is placed on top as it has higher potential than gate. Generally

the bulk or substrate terminal of NMOS and PMOS devices are connected to ground and supply respectively.

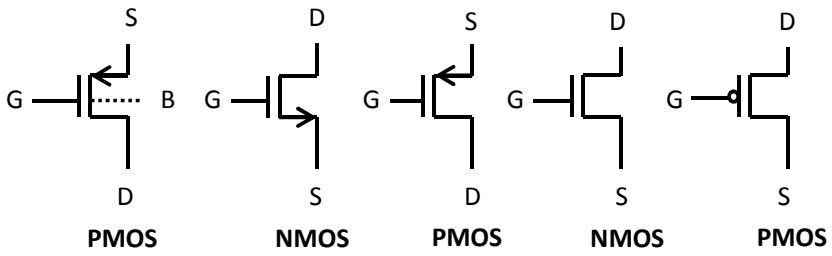
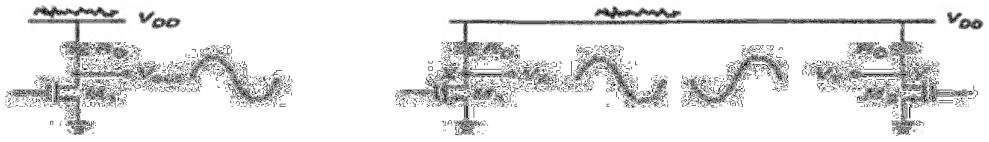


Figure 3.4 MOS Symbols

Differential Amplifiers is one of the most flexible circuits in analog circuits and very congenial with IC technology. It serves as input of the amplifier to permit input voltages to move around so that biasing of gain stage remain unaffected. It is a basic building block of analog CMOS circuit design. Differential amplifier can be classified into two ways:

3.3 Single Ended and Double Operation: When the outputis measured with respect to ground then the operation is called Single ended. A double ended or differential output is measured between two equal and opposite nodes centred about fixed signal known as common mode signal.

The advantage of double ended over single ended is higher immunity to noise can be understood from figure 3.5 that is if the circuit is symmetric, noise on supply would affect the both the output in the same amount thus when differential output is taken by substracting one output from another then effect of noise get nullified and we get noise free output.



If Vdd changes by ΔV then Vout changes by same

Noise in Vdd affects Vx and Vy , but not Vx-Vy

Figure.3.5 Immunity to Noise signal

In order to understand immunity of differential signal to noise, let us consider two adjacent lines in a circuit carrying a small signal and clock signal. Now, if there is some change in signal at line L_2, then due to capacitive coupling signals on line L_1 also get disrupted. But if we distribute a small signal in equal and opposite phase on two lines. Also if the clock line is introduced midway between two signals, then transitions distorts the differential signal equally keeping the same difference. Since common signal of two lines get corrupted, leaving the differential signal intact, therefore we can say this configuration rejects common mode signal or noise. Figure 3.6 illustrate the effect coupling on lines

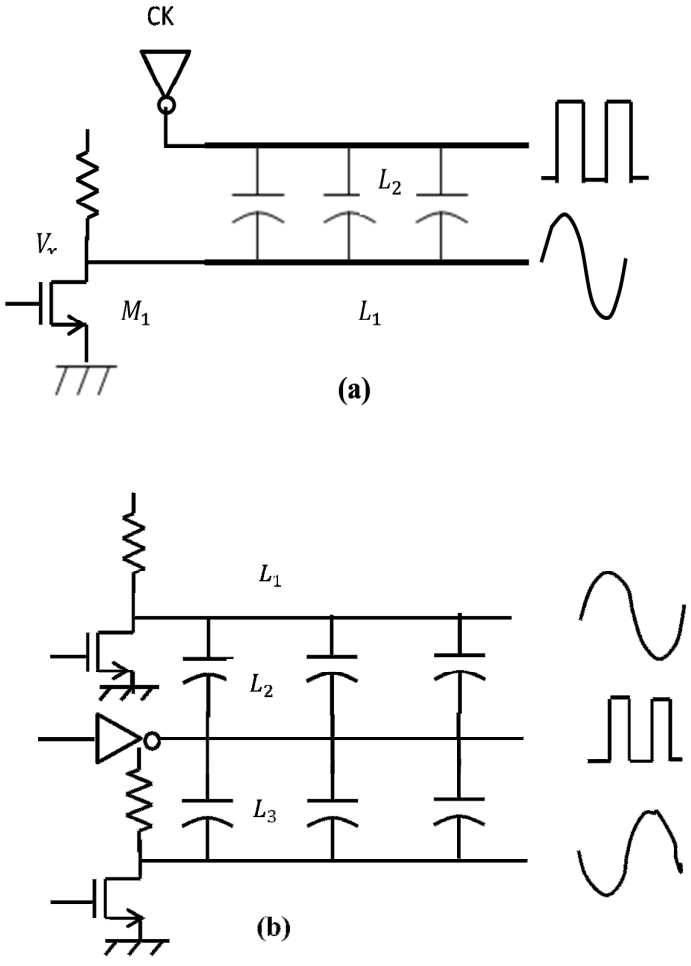


Figure.3.6 (a) Corruption of a signal due to coupling (b) Reduction of coupling by differential operation.

Different Topologies of Differential Amplifier:

1. Current Mirror Load Differential amplifier
2. Source degenerated resistive feedback
3. Split signal Differential amplifier
4. Resistive Common mode feedback Differential amplifier
5. Resistive Feedback and cross coupled differential amplifier
6. Cascode Differential Amplifier
7. Positive feedback cross coupled Differential Amplifier

3.4. Current Mirror Load :

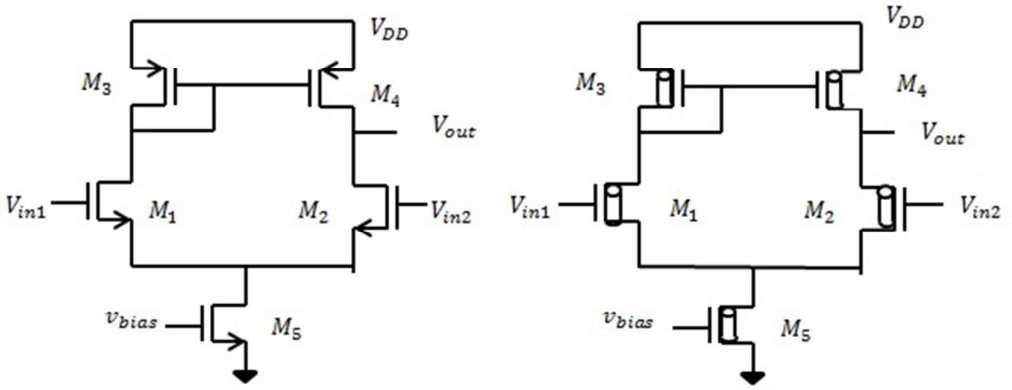


Figure.3.7 Current Mirror Load

This is the classical differential amplifier with current mirror load .The NMOS tarnsistors M1 and M2 form differential pair, M3 and M4 are PMOS load transistors which form current mirror.M5 is used as biasing source. All the transistors are said to operate in the saturation region. When the inputs V_{in1} and V_{in2} are applied respectively to the gate terminals of M1 and M2 , then differential input is given by:$V_{id}=V_{in1}-V_{in2}=V_{gs1}-V_{gs2}$.The gate of M3 is shorted to its drain terminal so that it acquires a constant value because I_{d3} and V_{gs3} are dependent on each other. The output is taken at the drain of M2 and from small signal analysis, output is given as

$$V_{out}=\{g_m(r_{04}||r_{02})\} \quad (3.1)$$

3.5 Source degenerated resistive feedback: In this topology resistance Rs provides degenerative resistive feedback. The degenerated resistors give negative feedback and it is required that current in both branches should be same for constant gate vo V_{dd} regarding of variation in the aspect ratio of M1 and M2 .By applying Kirchoff's Voltage Law at the input of differential pair, we get -: $V_{gs1}+ I_{d1}R_s$-$I_{d2}R_s$-V_{gs2}

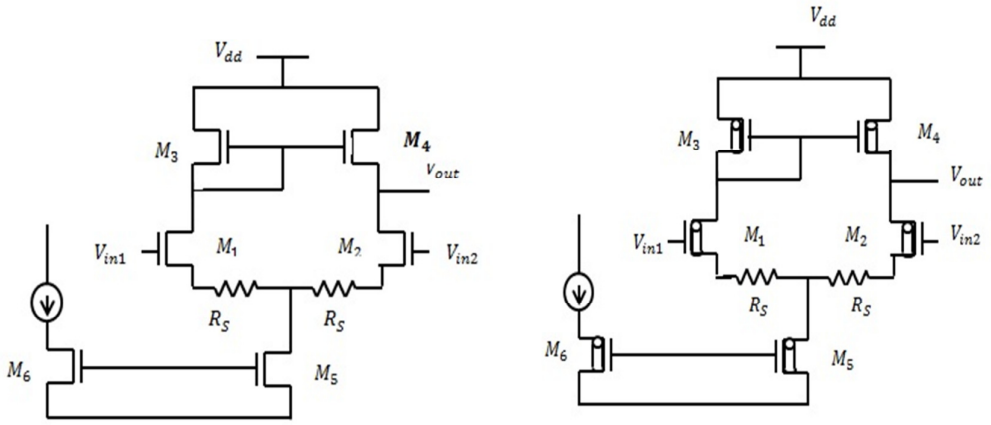


Figure.3.8 Source Degenerated Resistive Feedback

By differentiating above equation w.r.t aspect ratio of M2 and placing $g_m$in place $(\partial I_d/(\partial V_{gs})$, we get (∂Vgs1)/(∂Vgs2) = (1+Rsgm2)/(1+Rsgm1). From above, it can be stated that the both currents will be same due to negative feedback for any change in aspect ratio of transistors. Degenerative resistive feedback is used to provide greater input range of the amplifier but output swing get degraded.

3.6. Split signal differential amplifier:

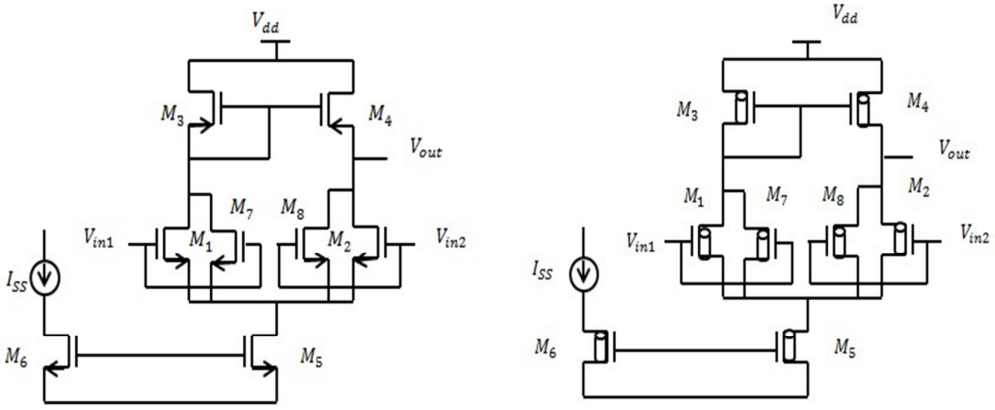


Figure 3.9. Split Signal Differential Amplifier

In differential amplifier the output voltage changes even for smaller amount of mismatch and therefore drive M2 and M4 out of the saturation region. One of the technique which could be adopted in order to minimize these variations is possibly splitting or dividing of signal transistors. The input transistors M1 and M2 are splitted into M1, M7and M2, M8.It has been assumed that transistors with low mismatch will ultimately minimize the effect of a higher mismatched transistor. The dependence of voltage on aspect ratio can be given by:

$$\frac{K_p(\frac{w}{l})_4}{2}(V_{GS4}-V_{tp})^2(1+\lambda V_{SD4}) = (1+\lambda V_{DS2})\frac{K_n}{2}[(\frac{w}{l})_2+(\frac{w}{l})_8](V_{GS2}-V_{tn})^2 \quad (3.2)$$

3.7 Resistive Common mode feedback:

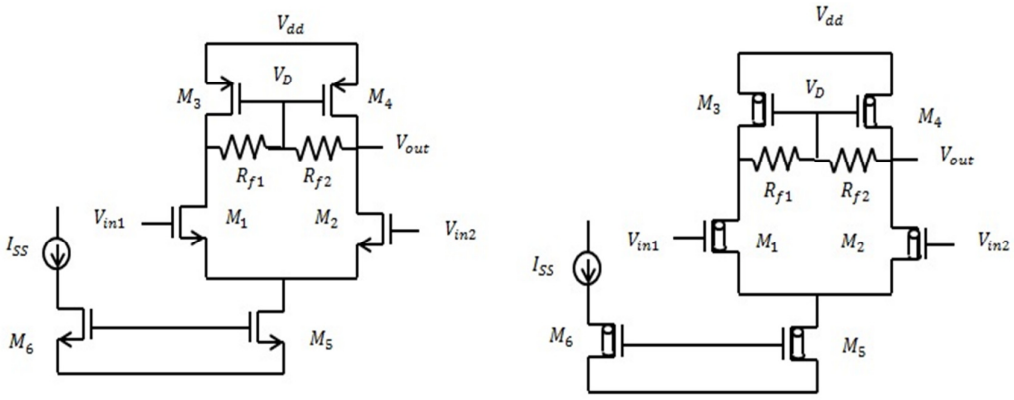


Figure. 3.10 Resistive Common mode Feedback Differential Amplifier

It has been observed that for very small deviation in voltage at the mirrored node there is a wide range of device mismatch whereas output is varied drastically even for small change in aspect ratio. In order to control the large output drift, resistive common mode feedback has been incorporated where resistors R_{f1} and R_{f2} provide common mode feedback path.The values of R_{f1} and R_{f2} will decide acceptable range of aspect ratio variation and influences gain of the circuitry. Assuming $R_{f1}= R_{f2}$, the gain will be given by

$$A_v= g_{m1,2}(r_{01,2}\|r_{03,4}\|R_f) \quad (3.3)$$

When compared with classical differential amplifier gain is constant for wide range of transistor mismatch, however value of gain and CMRR is reduced.

3.8 Resistive feedback with cross coupling

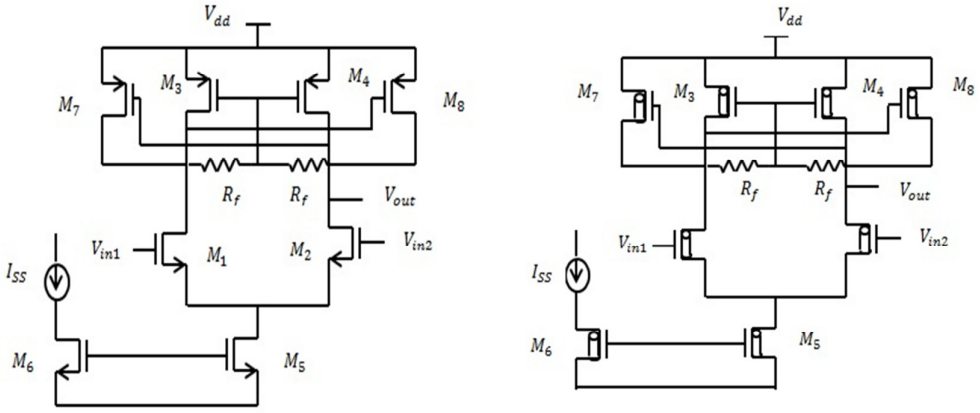


Figure 3.11 Resistive feedback with cross coupling

By common mode resistive feedback topology the effects of transistor mismatch get mitigated, though gain is degraded. In order to compensate this cross coupled pair has been used in this new topology. Transistors M7 and M8 provide negative resistance load to the amplifier and thus enhances the gain which depends on the ratio of g_{m7} and R_f.The gate voltage of M7 and M8 also changes and therefore cannot handle for large ratio variation.

3.9 Cascode differential amplifier

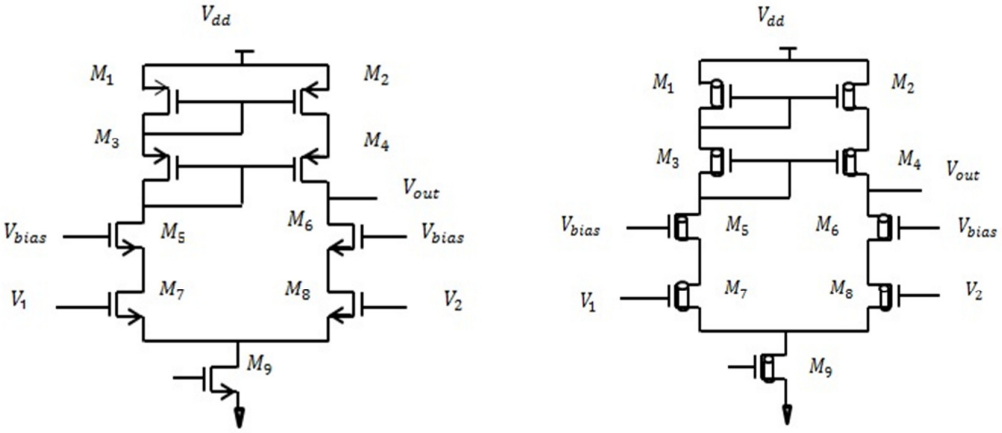


Figure 3.12 Cascoded Differential Amplifier

It has a high gain because of two mechanisms: one is the use of the current mirror and second because of the cascading transistors. The current mirror mechanism would produce a sharp input-output relationship. The cascading makes the I-V curves very flat which would further make the gain higher. The telescopic cascode is a

differential version of the Cascade amplifier. Its gain is in comparison to the two stage op-amp. It has high output impedance. It require a higher supply voltage than a two stage opamp. The output stage is high impedance, so the dominant pole is at the output. Compensation is provided by the load capacitance. So a minimum value of load capacitance is required for stability. The output common mode voltage is different from the input common mode voltage range. This presents difficulties in direct coupling to the next stage and DC feedback to its own input.

3.10 Positive Feedback Differential Amplifier:

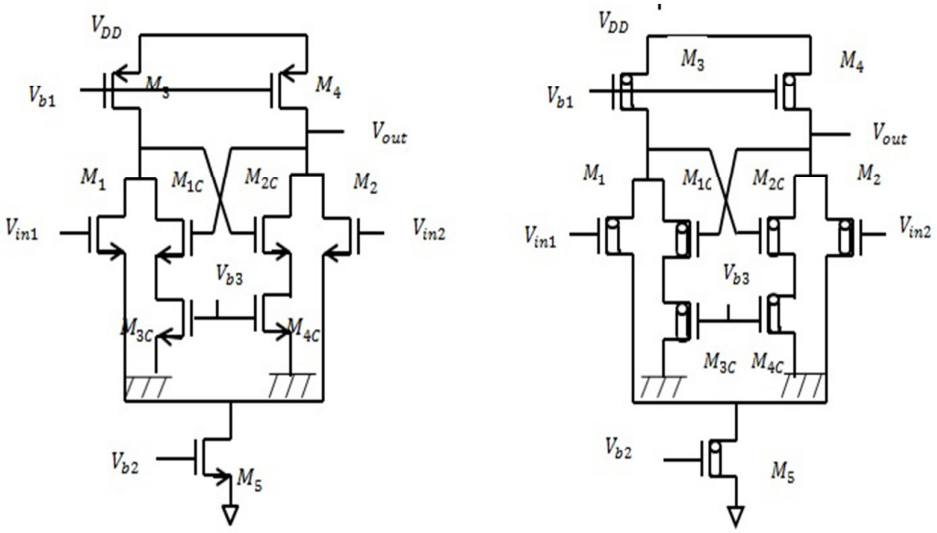


Figure 3.13 Positive Feedback Differential Amplifier

Positive Differential amplifier consist of positive feedback path between input and output. Positive feedback helps to increase the gain of the circuit as it provide infinite loop gain in ideal case. In CMOS differential amplifier circuit, the positive feedback path gives negative transconductance which cancel out the effect of positive transconductance generated due to NMOS and PMOS pair. Beside this cross coupled logic has been employed which further improves performance of the circuit. Transistors M_1,M_2 are input NMOS pair which takes the input signal,M_3 and M_4 are PMOS load pair which are biased with V_{b1},M_5 provide bias current for entire circuit for V_{b2} voltage. Complementary transistors M_{1C},M_{2C},$M_{3C}$and M_{4C} form feedback circuit and $V_{DD}$is supply voltage.

3.11 Large Signal Analysis of Basic Differential Pair:

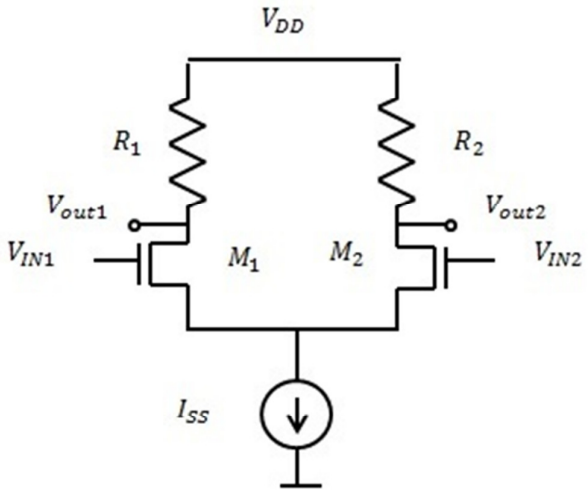


Figure 3.14 Resistive Load Differential Amplifier

Let us assume $V_{in1} - V_{in2}$ varies from - ∞ to + ∞.If V_{in1} is much less than V_{in2},Q1 is off,Q2 is On, and current through R2 i.e $I_{D2} = I_{bias}$ .Thus V_{OUT1}=$V_{DD}$and V_{OUT2}=V_{DD}-$R_D I_{SS}$ .As V_{in1} approaches V_{in2},M1 slowly turns on, taking some part of Issfrom R1 and hence reducing V_{out1}.Since I_{d1} + I_{d2}= I_{ss}, the drain current of Q2 decreases and V_{out2} increases.

For V_{in1}=V_{in2}, we have V_{out1}=V_{out2}=V_{dd}-$R_d I_{bias}$/2. As V_{in1} becomes more positive than V_{in2}, Q1 carries a larger current than does Q2 and V_{out1} falls below V_{out2}.For large V_{in1}−V_{in2}, Q1 take all of Ibias,turning Q2 off. As a result,V_{out1}=V_{dd}-$R_d I_{bias}$anV_{out2}=V_{dd}.Following Fig 3.14 shows the variation of both drain currents with input voltages

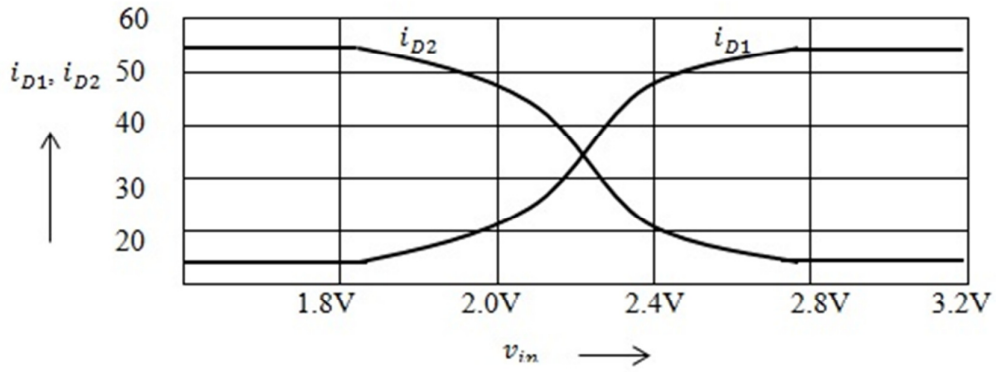


Figure 3.15 Variation of Drain current with Input voltage

Following two attributes can be revealed about Differential Pair:

I. The upper and lower levels at the output are well defined and are independent of the input common mode level.

II. The small signal gain i.e the slope between $Vout1 - Vout2$ and $V_{in1} - V_{in2}$ is maximum for V_{in1}=V_{in2}, subsequently falling to zero as $|V_{in1} - V_{in2}|$ increases or we can say the circuit becomes more nonlinear as the input voltage swing increases. For $V_{in1} = V_{in2}$, the circuit is in equilibrium.

We have V_{out1}=V_{dd}-$R_{d1}I_{d1}$ and $V_{out2} = V_{dd}$-$R_{d2}I_{d2}$, i.e V_{out1}-V_{out2}=$R_{d2}I_{d2}$-$R_{d1}I_{d1}$=$R_d(I_{d2}$-$I_{d1})$ if R_{d1}=R_{d2}=R_d.Thus we simply calculate I_{d1} and I_{d2} in terms of $V_{in1}$and V_{in2},assuming the circuit is symmetric,Q1 and Q2 are saturated .Since the voltage at node P where sources of Q1 and Q2 connected is equal to V_{in1}-V_{gs1} and V_{in2}-V_{gs2}.

$$V_{in1}\text{-}V_{in2} = V_{gs1}\text{-}V_{gs2} \tag{3.4}$$

For a square-law device, we have:

$$(V_{gs} - V_{th})^2 = \frac{Id}{0.5\mu nCoxW/L} \tag{3.5}$$

And, therefore,

$$V_{gs} = \sqrt{\frac{2I_d}{\mu Cox\frac{w}{l}}} + V_t \tag{3.6}$$

It follows from above equations,that

$$V_{in1}\text{-}V_{in2}= \sqrt{\frac{2I_{d1}}{\mu Cox\frac{w}{l}}} - \sqrt{\frac{2I_{d2}}{\mu Cox\frac{w}{l}}} \tag{3.7}$$

Our objective is to calculate the differential output current, I_{d1}-I_{d2}. Squarring the two sides and knowing I_{d1}+I_{d2}=I_{ss}, we obtain

$$(V_{in1} - V_{in2})^2 = \{\frac{2}{\mu Cox\frac{w}{l}}\} (I_{ss}\text{-}2\sqrt{I_{d1}I_{d2}}) \tag{3.8}$$

That is,

$$\frac{1}{2}\mu Cox\frac{w}{l}(V_{in1} - V_{in2})^2\text{-}I_{ss}= -\ 2\sqrt{I_{d1}I_{d2}}. \tag{3.9}$$

Squarring the two sides again and noting that

$4I_{d1}I_{d2}=(I_{d1}+I_{d2})^2-(I_{d1}-I_{d2})^2=I_{ss}{}^2-(I_{d1}-I_{d2})^2$,

we arrive at

$$(I_{d1}-I_{d2})^2=-1/4(\mu c_{ox}\frac{w}{l})^2\{(V_{in1}-V_{in2})^2\}^2+I_{ss}\mu c_{ox}\frac{w}{l}(V_{in1}-V_{in2})^2$$

Thus,

$$I_{d1}-I_{d2}=1/2\mu c_{ox}w/l \qquad (3.10)$$

3.12 Various Parameters: There are parameters on the basis of which performance any differential amplifier can be analysed and these are:

3.12.1 CMRR: The ability of differential amplifier to reject common mode signal applied to both the inputs is known as Common Mode Rejection Ratio. If we apply an AC signal v_c to the gates of M1 and M2 ,we can calculate common mode gain by the formula:

$$A_c=\frac{v_o}{v_c}=\frac{-1/gm3,4}{2Ro}$$

Effect of common node noise on signal can be observed from figure 3.15

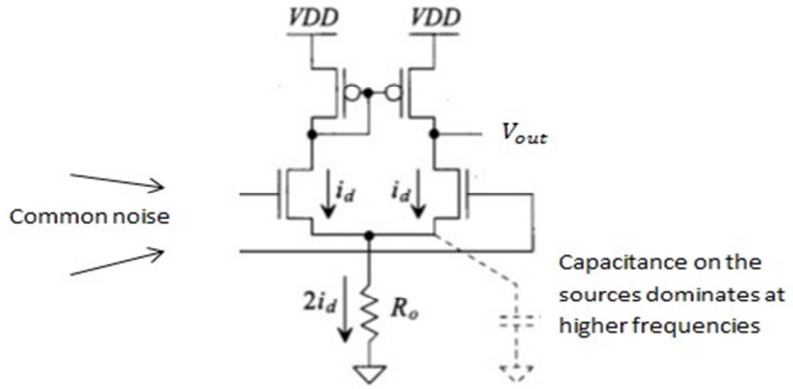


Figure3.16 Effect of Common noise on output signal

Common mode gain decreases by increasing the value of biasing current source output resistance. CMRR in db can be given by:

CMRR=20log[$g_{m1,2}(r_{02}\|r_{04})2g_{m3}$,$4R_0$]

Larger the CMRR, better the performance of the diff amp

3.12.2 Input-Referred Offset-It is a minimum voltage that should be applied at both the inputs so that there is less sensitivity output voltage variation with change in input common mode voltage. Figure 3.15 shows the variation of output w.r.t input

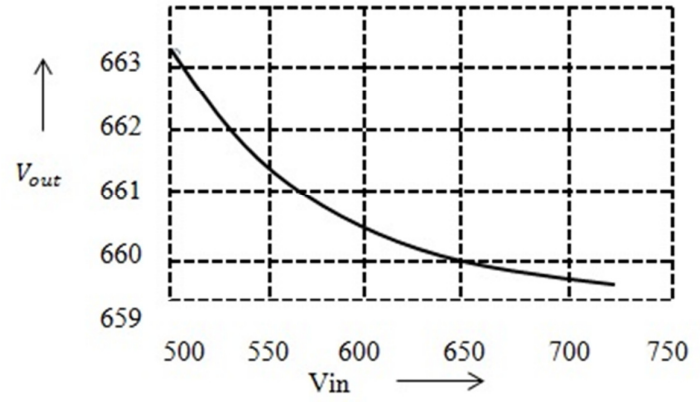


Figure 3.17 Variation of Output voltage with Common mode voltage

3.12.3 Differential Gain and Common mode Gain: The output voltage of an amplifier at DC can be represented as: $V_O = A_{od}(V_2 - V_1) + \frac{A_{ocm}}{2}(V_1 + V_2)$ where A_{od} and A_{ocm} are differential and common mode gains respectively of operational amplifier at dc. For an amplifier with a finite CMRR, $A_{ocm} = A_{od}$/CMRR

3.12.4 Slew Rate: Slew rate is defined as rate at which output voltage changes with time for a given change in input voltage. In the figure 3.16 for a given current mirror load differential amplifier slew can be calculated when either M1 or M2 turns off, then the total current available to charge or discharge a load capacitance is given by Iss. This current can then help to drive the next stage. For high speed , we need large bias current

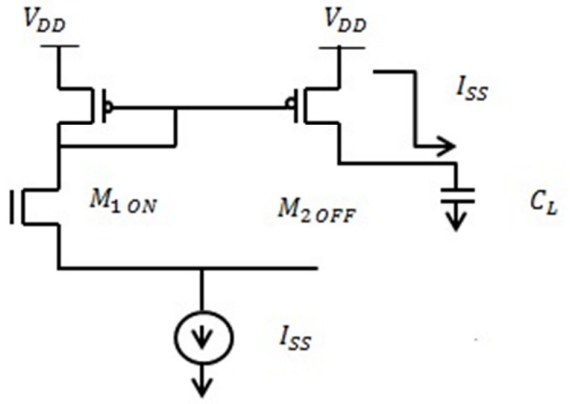


Figure 3.18 Charging and discharging of Output Capacitance

3.12.5 Unity-Gain Frequency: The 3db frequency $f_b$and the unity gain frequency or gain-bandwidth product f_t of an amplifier are related through

$$\mathbf{f_b = \frac{f_t}{A_{od}}}$$

3.12.6 Output Resistance (R_o): It is the resistance seen at the output terminal of an operational amplifier.

3.12.7 Differential Input Resistance (R_{id}): The resistance present two input terminals that is inverting and non inverting of the amplifier is known as differential input resistance.

3.13 Positive feedback: Positive feedback is a technique which is employed in analog circuits in which a part of output signal returns to the input and is in phase with it, the circuit gain increases. A simple feedback loop is shown where loop gain AB is positive, also called as regenerative or positive feedback. Transfer function can be given by:

T = A/(1-AB)

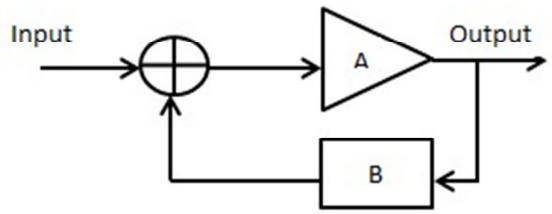


Figure3.19 Block diagram of Positive Feedback Circuit

The loop gain values must be greater than zero but less than one to ensure the feedback is positive. When the AB is equal to one, the denominator becomes 0, thus transfer function becomes ∞.At this point, the pole shift towards the right half plane and circuit becomes unstable.

Positive feedback differential amplifier: This configuration make use of cross coupled MOS transistor that feedback between the input and the output nodes. The feedback circuit generates a negative transconductance which cancels the positive output conductance generated by NMOS differential pair and PMOS load ,thus increasing the overall gain and output swing.

Positive feedback amplifier consist of current source PMOS load pair M3 and M4 whose gates are biased by some external voltage.M1 and M2 are NMOS input differential pair on which both inputs are applied. Transistors M1c, M2c, M3c and M4c form positive feedback path where M1c and M2c gates are cross coupled with output. Due to this cross coupling any change in output swing will immediately change the potential at the gates of M1c and M2c hence varying the gain of the circuit. One new feature of the circuit is bias voltage Vb2 which is exclusively provided to adjust the gain accordingly.Vb2 is connected to the gate of both M3c and M4c to keep them in saturation. For different values of Vb2 different output resistance can be obtained at the drain of cross coupled transistors which in turn can give different gain. Transistor M5 is used as a biasing source to which bias voltage Vb3 is applied.

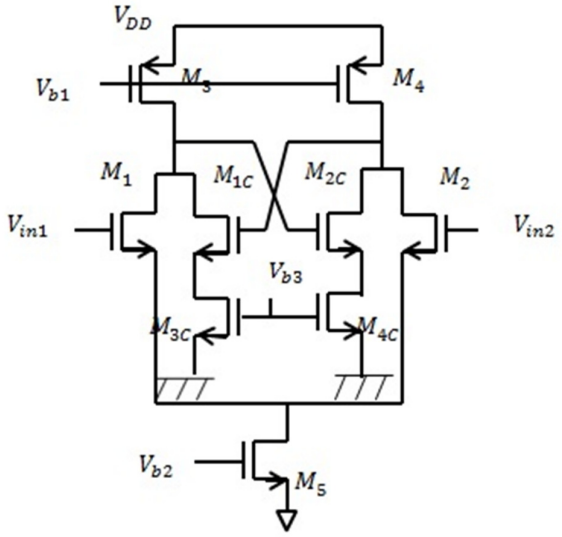


Figure 3.20 Positive Feedback cross coupled differential amplifier

Small Signal Analysis:

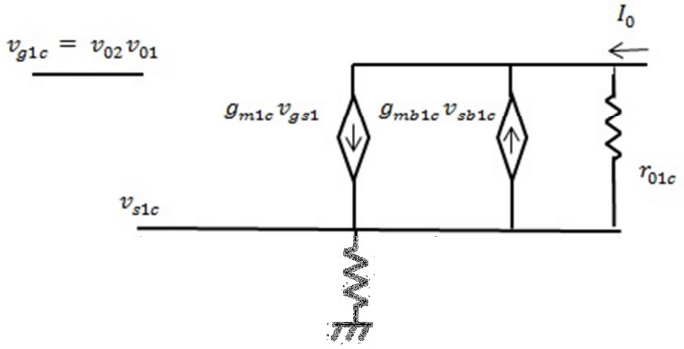


Fig 3.21 Small signal model of Positive Feedback Differential Amplifier

Short circuit transconductance can be given by:

$$G_m=I_0/V_{glc}=I_0/V_{02} \quad (3.11)$$

By using small signal model of cross couple MOSFET, transconductance can be given

$$G_m = \frac{g_{mlc}}{\frac{r_{01c}+r_{03c}}{r_{01c}} + g_{m1c}r_{03c} + g_{mb1c}r_{03c}} \quad (3.12)$$

R can be defined as

$$R=V_{01}/I_0=V_{01}/G_mV_{02}= -V_{02}/G_MV_{02}= -1/G_m$$

Output resistance

$$R_0=V_t/i_t=r_{01c}+r_{03c}+(g_{m1c} + g_{mb1c})r_{01c}r_{03c} \quad (3.13)$$

Thus, the overall transfer function is:

$$A_d=\frac{V_{02}-V_{01}}{V_{id}} = g_{m1}(r_{01}||r_{03}||R_0||R) \quad (3.14)$$

It can also be written as:

$$A_d = \frac{V_{02}-V_{01}}{V_{id}} = \frac{g_{m1}}{\frac{1}{r_{01}}+\frac{1}{r_{03}}+\frac{1}{R_0}-G_m} \quad (3.15)$$

In positive feedback minimum voltage swing is same as that of basic differential amplifier but maximum voltage swing is higher because p channel MOSFET require to lower by only overdrive voltage that is Vmax =Vdd -Vov. Thus increasing the overall range of voltage swing.

3.14 Limitations of Cmos at nanoscale : One of the striking feature of CMOS technology is great potential of scaling size of MOS transistors. Ideal scaling theory obeys some rules: (a) decrease all vertical and horizontal dimension by factor k (k>1); (b) reduce the supply and threshold voltage by same k; (c) increase the doping level by k.

The scaling of device has following effects on MOS transistors physics:

- Total Channel capacitance decrease by k
- Power dissipation reduces by k^2
- Current carrying capability decreases by factor k

- Total supply voltage drops by k
- Maximum voltage swing reduces by k
- Electric field remains constant

Usually technology scaling is slightly different from ideal scaling. The threshold and supply have not decreased as the same level as device dimensions. Moreover, many short channel effects become prominent thus making it little challenging.. For hand calculations in MOS device, the model which is used is square . Law but it does not take into consideration second order effects .These effects are mainly due to small channel dimensions which is an important property of nano devices. In order to tackle these short channel effects we require more advanced model like BSIM4v4 model which provide good performances for devices working at submicron level. Submicron operation faces problems like

- Process variation
- Higher gate-oxide leakage
- Low output resistance
- lowtransconductance
- high sub-threshold conduction
- heat generation

3.14.1 Process Variation: With continuous reduction in size of MOS device,the number of silicon atoms present also decreases thus changing various properties of the transistor which causes unpredictability in the placement and control of number of dopants. Besides this, while fabricating the device various variations of random nature distorts the transistor size i.e. width, length, thickness of oxide etc. which become large fraction of transistor size as a whole. All these fluctuations leads to an unfavourable design.

3.14.2 Higher gate-oxide leakage: Gate oxide which acts as an insulator between channel and gate must be very narrow in order to enhance the conductance and performance of the channel during ON mode of transistor and reduce the sub threshold leakage during OFF mode. In oxide thickness of about 1.2nm (equivalent to thickness of

5 atoms in silicon), quantum tunnelling phenomenon starts functioning between gate and channel that results in rise of power consumption. An insulator which possesses higher dielectric constant than that of silicon like oxides of zirconium can be effective in reducing the gate leakage. Also a thicker dielectric can reduce the current due quantum tunnelling passing through gate oxide present between gate and channel.

3.14.3 Low Output Resistance: In analog circuits for higher gain, a high output resistance is required i.e. variation of output current should be very low with the drain to source voltage. With minimization of device size, the effect of drain become approximate to that of gate due to the rising proximity between gate and drain which increases the reactivity of the MOS current for drain current. To compensate the resulting fall in output impedance, intricacy of the circuit has to increase by employing more number of devices , for example cascode circuit or providing a feedback circuit by using operational amplifiers.

3.14.4 Low Transconductance: The transconductance of the MOS device helps in determining its gain and depends largely on mobility of holes and electrons specially for lower drain voltage. Decrease in device size leads to higher electric fields around channel region with increase in impurity levels of the dopants. When dimension of channel along source to drain region decreases not in proportion with drain voltage, then electric field of the channel increases and results in carrier velocity saturation thus limiting the current and transconductance.

3.14.5 High Subthreshold Conduction: When geometries of MOS device reduces, then in order maintain the performance of the circuit threshold voltage has to be decreased. For lower threshold it become tough to change the transistor state from OFF to ON as available voltage swing is less. Therefore circuit design is all about taking a middle way between high current during ON state and low current during OFF state.

In circuit, most of the power get consumed in sub threshold leakage which is due to leakage through reverse bias junction and gate oxide.

3.14.6 Heat generation: Due to increase in density of number of MOS devices on a single chip, large amount of heat get generated which can harm the circuit. With such alarming temperature inside the circuitry, operation of circuit becomes slow, life of circuit reduces and its consistency also degrades. In order eradicate the excess heat

various cooling devices and heat sinks are introduced in the integrated circuits. When even these heat sinks failed to work properly, the temperature at the interconnects may rise up hysterically, thus damaging the device.

3.15 MOS SPICE models: MOS models which have been used so far made significant progress in improving accuracy as device dimensions reduces to submicron. But in order to estimate the behaviour of circuits more accurately, SPICE simulators need an accurate model for MOS transistor simulations. Till now, various models with distinct features and parameters for short and long channel devices have been used. The selection of a particular model for NMOS and PMOS depends on process technology. Generally IC manufacturer is required to provide model.

The basic MOS transistor model is level 1 which does not take into consideration short channel effects. This level provides significant accuracy for channel lengths as small as 4µm.

Next in the series is level 2 which give good accuracy for small devices working in saturation with L~0.7µmbut it give substantial error for output impedance and switching point between triode and saturation regions. Moreover for narrow and long devices, model is not accurate. Level 3 features are more or less same as level 2 with some additional empirical constant used to improve upon accuracy for channel length as small as 1µm. An noting drawback of the model is that it shows discontinuity of derivatives of I_D w.r.t V_{ds}at the edge of the triode region which creates problem while measuring output impedance.

Other commonly used MOS model by chip designers is the Berkeley Short-Channel BSIM model. For past few years, BSIM models have been set as the de facto standard SPICE model for MOSFET and CMOS technologies. The concept behind LEVEL 1, LEVEL 2 and LEVEL 3 was to express behaviour of device with the help of equations. But BSIM model adopted different approach. It incorporates simple equation to demonstrate geometry dependence of many device parameters. The equation is of the form:

$$P = P_0 + \frac{\alpha_p}{L_{eff}} + \frac{\beta_p}{W_{eff}}$$

Where P_0 is the parameter for long, wide transistor and α_p and β_P are fitting factors.

BSIM model includes around 50 parameters. Its performance for narrow, small transistors is not so good. It provides negative output impedance at high drain source voltages for saturated MOSFETs. Moreover in deep triode region, BSIM shows slight discontinuity in drain current. The next model in series is BSIM2 which incorporate around 70 parameters. This version includes new equations for mobility, sub-threshold conduction and drain current. Its advantage over BSIM is that it provides output impedance more accurately.BSIM2 faces larger errors in triode region and substantial problems in the saturation region.

Modelling the device behaviour with empirical equations ignoring physical phenomena makes it difficult for short channel devices. In order to overcome the shortcoming of previous series, BSIM3 has utilized physical principals to improve device performance.BSIM3 includes 180 parameters and works for channel lengths of approximately 0.25µm.This model provide accurate results for strong inversion and sub threshold operation. The next generation of it is BSIM4, which shows major improvements over BSIM3v3 like

- Flexible substrate resistance
- Accurate channel thermal noise and noise partition model for induced gate noise
- A comprehensive and versatile geometry dependent parasitics model for source/drain connections and multi finger devices.
- A more accurate mobility model for predictive modelling
- Accepts either the electrical or physical gate oxide thickness as the model input in a physically accurate manner.
- A gate induced drain leakage current model, not available in earlier BSIM models.
- Different diode IV and CV characteristics for the source and drain junctions.
- A dielectric constant of the gate dielectric as a model parameter
- .OPTION LIST now prints the total capacitances, instead of just the intrinsic capacitances for the BSIM4 (level 54) MOSFET model.

3.16 HSPICE – Analog simulation tool

HSPICE is SPICE based simulation tool which is popularly used in industry for performing numerical convergence, assists the latest device and offer measurments and optimization of circuits. The acronym SPICE depicts Simulation Program with Integrated Circuit Emphasis. When circuit to be simulated is formatted in a special syntax (HSPICE net list syntax) with defined supply sources, then numerical routine will do the analysis and represent numerical or graphical results desired by user. This simulation basically involves three steps:

- Generating netlist of the circuit
- Running Simulation
- Printing and analysing the simulation results

For generating netlist any text editor software with extension (i.e. filename. sp) can be used and is composed up of statements incorporating circuit components, interconnections, device models, input signals, voltage and current sources, type of analysis(i.e. DC, AC, Transient) and output data format. In general netlist file structure is as follows:

Title (mandatory)

Circuit description

Sub-circuit description (optional)

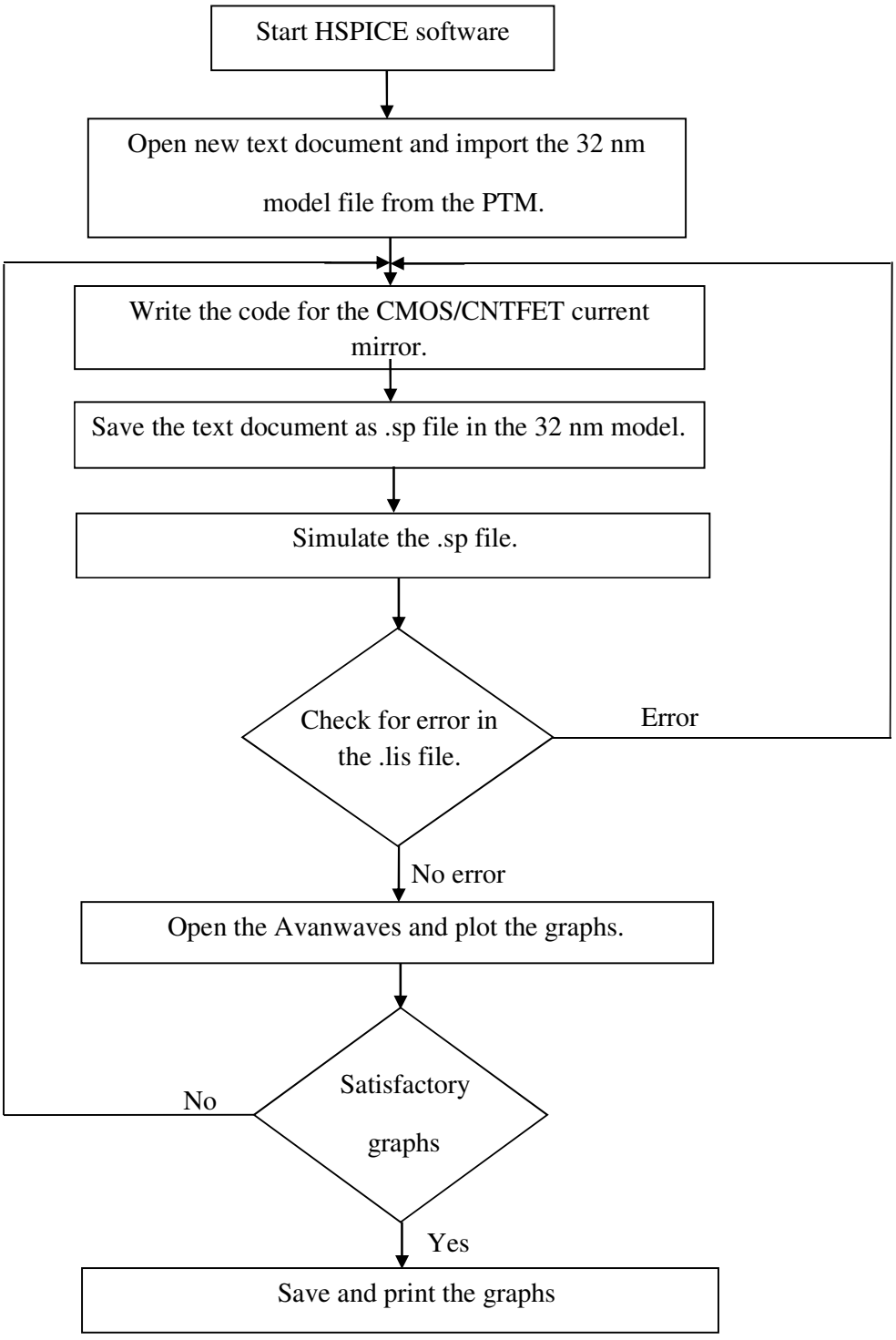
Device models

Analysis

Output Format

.end (mandatory)

3.16.1 FLOW CHART



3.17 CARBON NANOTUBE

As CMOS technology have to dealth with many challenges at nanoscale like short channel effects, tunnelling, higher leakage power there is a requirement of some better alternative which could perform well at these small dimensions sustaining Moore's Law. In this domain, from past few decades CNTFET seeking lot of attention as it shows some exceptional characteristics like high mobility, near ballistic transport, low junction capacitance, high current driving capacities. All these characteristics are very much desired for enhancing the performance of analog circuits.

There are four types of naturally occurring carbon like Graphite, Diamond, ceraphite and fullerenes. Carbon nanotubes are made by rolling up graphene sheets into a tubular structure at different angles. These cylindrical tubes can be single walled or multi walled proportional to the number of shells that make these tubular structures. Single walled consist of one shell of carbon atoms and multi walled comprises of multiple shells of atoms as can be seen in figure 3.20. It uses either a single tube or number of nanotubes as a channel material in place of bulk silicon in conventional MOSFET.

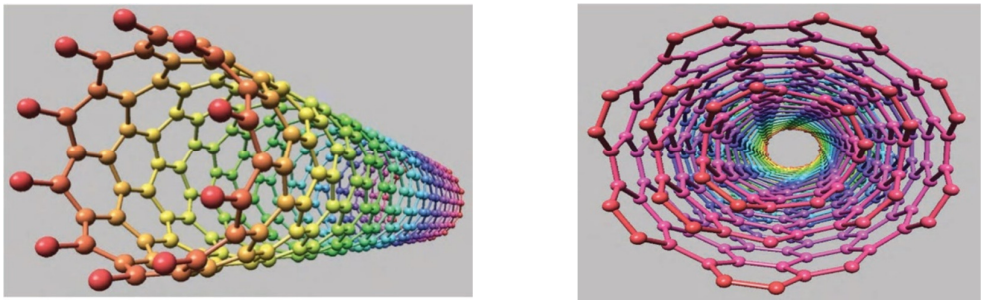


Fig 3.22 Single walled and Multi walled Carbon Nanotube

Studies have shown that semiconducting CNTs have extra ordinary electrical properties like long mean free path, high transconductance and high mobility which have great potential for sub nano regime. The principle of operation of CNTFET is more or less same as that of MOSFET.CNTFETs embodies an 1D FET with its narrow cylinder confines electrons in one direction with backward and forward movement, whereas in case of MOS it is 2D FET where electrons are free to move in 2D plane. In CNTFET ballistic transport dominates while in MOSFET diffusive transport is in

operation. For ballistic CNFETs, linear region current can be estimated by the difference between source and drain moving carriers. In case of MOSFET current saturates at pinch off thus making drift velocity independent of drain voltage and in CNTFET current saturates when left moving carriers from drain vanishes, thus only right moving exist in channel. Improvement in contact resistance at drain and source terminals has further enhanced CNTFET performance. One of the important factor behind selecting CNT is their one dimensional structure due to which carriers are confined within the cylinder of the tube which give way to quantization of charge carriers. Moreover the I-V characteristics of CNTFET are alike to MOSFET .As it is known fact graphene has sp_2bond which is even stronger than diamond so therefore Carbon nanotubes show high mechanical, thermal and electrostatiscal strength. The electrical behavior of CNT is determined by chiral vectors.It has different denomination for different combination of m and n.

$$C_h = n a_1 + m a_2$$

where $a_1$and a_2 are unit vectors

If m and n are same then it is armchair, for (m, 0) pair the type is zigzag, otherwise it is simply chiral. These characteristics will define device as semiconductor or conductor. The most determining parameter of CNTFET is its diameter, which affects all other important parameters of the device like threshold voltage, energy bandgap, transconductance etc. with increase in diameter, gain of the circuit decreases whereas power consumption and bandwidth increases. Generally diameter in the rangefrom 0.7nm to 2nm is preferred for high performance of analog circuits. Diameter of CNTFET is given by:

$$D_{CNT} = \frac{\sqrt{(n_1^2 + n_2^2 + n_1 n_2)}}{\pi}$$

A Single Walled CNT is a conductor if n-m=3k ($k \in Z$),otherwise it is a semiconductor. Like MOSFET, CNTFET device has a threshold voltage (Vth) which is needed for making device ON via top gate. A unique feature of CNTFET is that by changing the chirality, one change control the threshold voltage as diameter is inversely proportional to bandgap which inturn determine the threshold by using formula:

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3} = \frac{a V_\pi}{e D_{CNT}} = \frac{0.43}{D_{CNT}(nm)}$$

Where a = 2.49A is termed as distance between two carbon atoms,V_π=3.033 eV is carbon π-π bond energy, e is the unit electron charge. Internal structure of CNT shown in figure 3.21 consist of CNT as a channel between drain and source terminal.

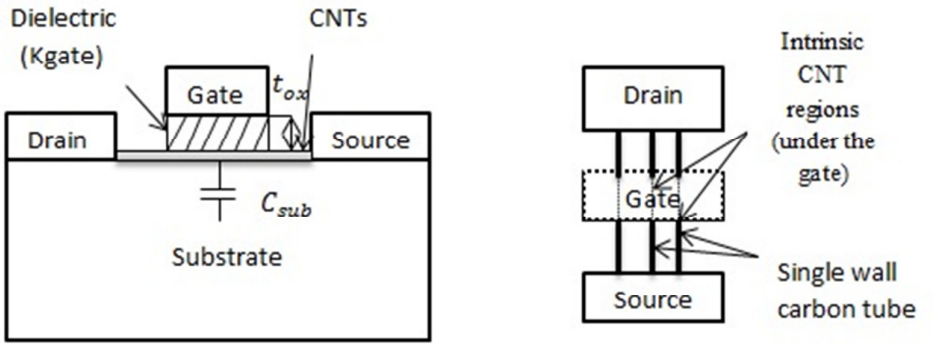


Figure 3.23 Internal Structure of Carbon nanotube

3.18 CNTFET SPICE MODEL: The viability of CNT-FET circuits depends on nature of devices that comprise multiple CNT transistors and form large scale circuits. Therefore device model is important to predict the CNTFET based circuits behaviour. Like CMOS models helped in optimization of CMOS circuits, it will be beneficial to optimize CNT circuits design by using CNTFET models. The Stanford CNFET Model is SPICE based compact model which includes enhancement-mode MOSFET, unipolar MOSFETs of semiconductor single-walled tubes(carbon nanotubes) as channels. Each device can have one or many number of carbon nanotubes of chirality as defined by user, and channel length scaling can be accurately modeled down to 20nm. The model considered quasi-ballistic transport and inculcated an accurate usage of the capacitor network in CNFET. It has taken into consideration several non-idealities, like scattering of carriers by acoustic and optical phonons capture in the nanotubes, effect of the parasitic capacitances between gate and source/drain terminals formed by many 1D nanotubes, phenomenon of the charge screening between the adjacent nanotubes, the access resistance of the source/drain extension regions, the Schottky-barrier resistance at the metal-nanotube contact interfaces, and the band-to-band leakage current. The model has been used to perform circuit-performance comparison with the standard digital library cells between CMOS random logic and CNFET random logic. In addition, by including a full transcapacitance network, it also produces better predictions of the dynamic performance and transient response. The CNFET model can

be instantiated directly in SPICE netlists to explore the impacts of CNFETs on the circuit performance. It is an accurate and handy tool for design exploration and verification of CNT circuits.

Table 3.1 Scope of the CNTFET Model:

Device Types	n-type/p-type CNFET
Device Dimensions:	
Channel Length (Min)	~10nm
Channel Length (Max)	Unlimited
Channel Width (Min)	4nm
Channel Width (Max)	Unlimited
Number of CNTs	1
Number of CNTs	Unlimited

This model has been designed for MOSFET type CNFET devices which consist of one or more number of carbon tubes.The minimum channel length limit which can be modelled here is 10nm as various mechanism which dominate at below 10nm are not described here whereas there is no maximum limit.However for channel length greater than 10nm are treated as long channel device, this transition from short to long channel is automatically handled by Stanford model.

3.19 Technology node: The scaling in technology is motivated by the number of factors like reducing the fabrication cost, decreasing the power dissipation, increasing the speed of operation, integrating large number of devices within given area.The naming of technology nodes (130,90,…32nm) comes from the international Technology Roadmap for Semiconductors (ITRS2009). Following table gives an overview of parameters like effective gate length, gate dielectric, gate materials etc for different technology nodes.

Table 3.2 Features of Different Technology Nodes

Technology Node	130nm	990nm	65nm	45nm	32nm
First production	2001	2003	2005	2007	2009
Effective gate length	70nm	50nm	35nm	30nm	25nm
Gate material	Poly	Poly	Poly	Metal	Metal
Gate dielectric	SiO_2	SiO_2	SiON	High K	High K
Memory point (μ^2)	2.4	1.3	0.6	0.3	0.17

The polysilicon continued to be used as gate material with silicon dioaxide as insulating material between gate and channel. Starting from 90nm technology SiON dielectric has replaced SiO_2 which gives higher permittivity and subsequently higher performance while maintaining low level of leakage current. The reduction in leakage current become significantstarting from 45nm technology node with the use of various high dielectrics like hafnium oxide, zirconium oxide or titanium oxide. In 32nm technology node manufacturer uses a combination of high K dielectric and metal gate.

With each lithographic scaling, the linear dimensions are decreased by a factor of 0.7 and area shrinks by factor of 2, which results into higher integration density when compared to previous technology node. Several 32nm processes have been introduced by various manufacturers for different applications. Variable transistor channel lengths in the range from 25nm to 32nm are provided by different manufacturers. On comparison to 45nm technology, 32nm node provide:

- 30% reduction in power consumption
- Twice the packing density
- 30% rise in switching performance
- Reduction of the leakage between source and drain and through gate oxide

Table 3.3 Values of different parameters for 32nm Technology

Parameters	Value
Vdd (V)	0.8-1.1 V
Effective gate length(nm)	25-35
Ion N(μA/μm) at 1V	1000-1550
Ion P(μA/μm) at 1V	500-1210
Ion P(nA/μm)	0.1-200
Ion P(nA/μm)	0.1-100
Gate dielectric	HfO_2,SiON
Equivalent oxide thickness (nm)	0.9-1.2
No of metal layers	6-11
Interconnect layer permittivity K	2.4-3.0

The above table 3.3 shows the values of different parameters which are used for 32nm Technology which consist of supply voltage, effective gate length, Gate dielectric material , oxide thickness, number of metal layers required etc. These values shows the admissible range which when taken care off can give the desired results for given technology node.

Results and Discussion

RESULTS AND DISCUSSION

In the previous chapter, the structure and characteristics of Differential amplifier using CMOS and Carbon Nanotube Field effect Transistor have been discussed.Since the main empphasis of the thesis is on finding the topology of differential amplifier which can give maximum gain and bandwidth.

All the CMOS and CNTFET devices are simulated and results have been categorically presented with the help of HSPICE simulation tool and using Stanford model of Carbon nanotube which includes effect of various parameters like chirality, dielectric constant, temperature and gate insulator thickness

Table 4.1 CMOS Differential Amplifiers at 32nm

	Differential amplifier with active load	Source degeneration differential amplifier	Multiple signal differential amplifier	Resistive common mode differential amplifier	Resistive cross coupled common mode feedback	Positive feedback Differential amplifier	Cascode Differential Amplifier
Power dissipation (mW)	219	218.7	225.9	219.9	236.4	235.4	258.7
Gain	9.3	8.87	11.85	3.58	11.63	16.4	14.4
Bandwidth (Ghz)	12.9	11.34	17	7.59	4.4	28.4	4.6
Phase Margin	103˚	104.8˚	95˚	124˚	149˚	91˚	94.6˚
CMRR	32.21	31.92	34.15	20.28	37.93	27.5	30.4

4.1 CMOS Differential Amplifier with active Load :

Transfer characteristics of CMOS differential amplifier with active load is linear in the range from -0.3V to +0.3V and in saturation region for other values of input voltage for given supply voltage.

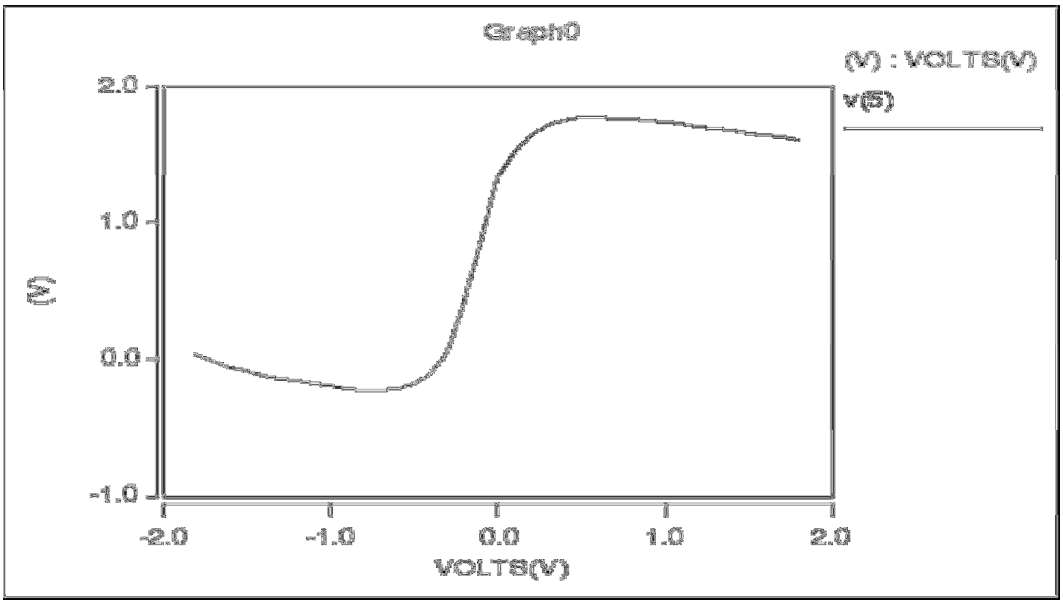


Fig 4.1 Transfer Characteristics of CMOS differential Amplifier with Active Load

Frequency Response Curve of CMOS differential Amplifier with active load provides bandwidth of 12.9 Ghz and gain of 9.3 db

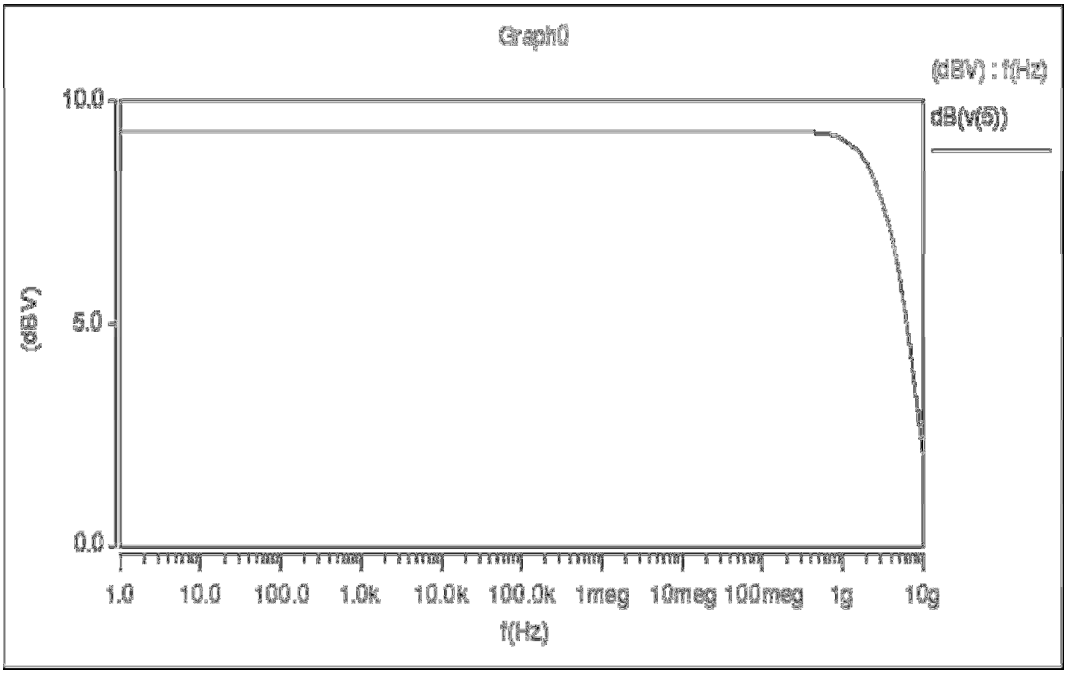


Fig 4.2 Frequency response curve of CMOS differential Amplifier with Active Load

Phase curve of CMOS differential Amplifier with active load gives phase margin of 103°.

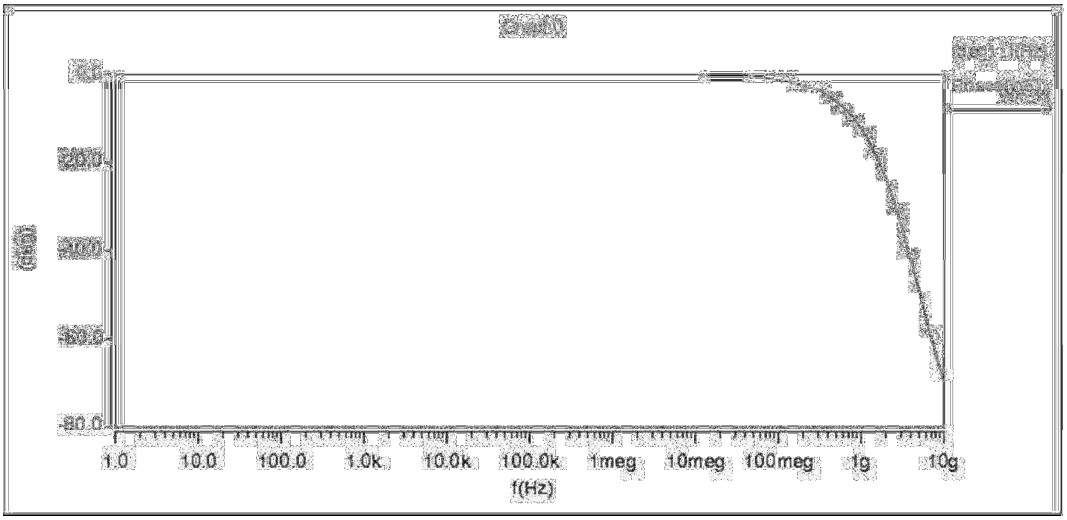


Fig 4.3 Phase Curve of CMOS differential amplifier with Active Load

4.2 CMOS Source Degeneration Differential Amplifier:

Transfer Characteristics of CMOS Source Degeneration Differential Amplifier shows that amplifier operates in linear region for values -0.4V to +0.4V and for values above or below this range either of the mosfet enter into non saturation

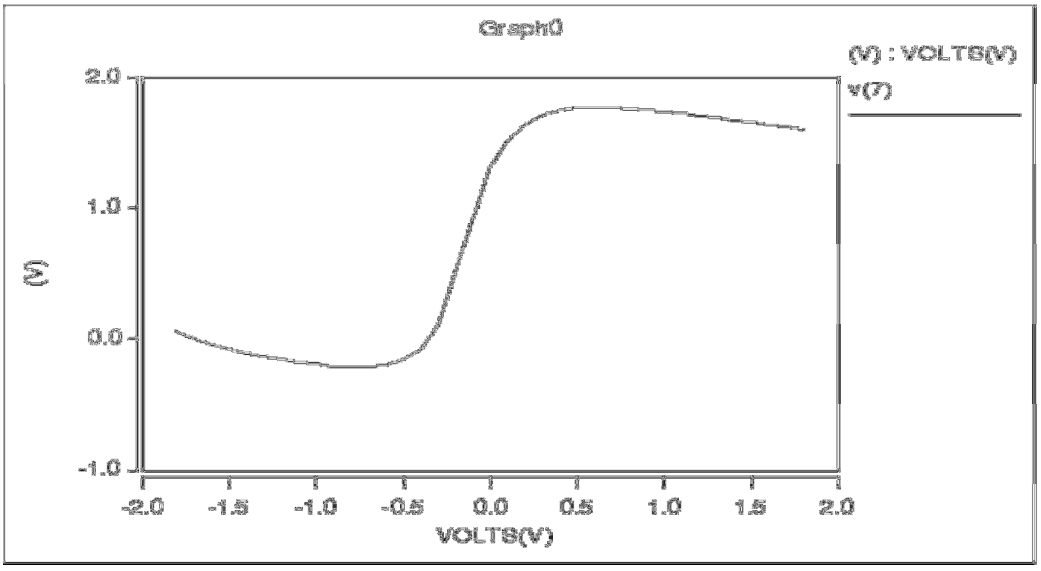


Fig 4.4 Transfer Curve of CMOS Source Degeneration Differential Amplifier

The Bandwidth of Source Degeneration is 11.34 Ghz and gain is 8.87 db as seen from frequency response curve.

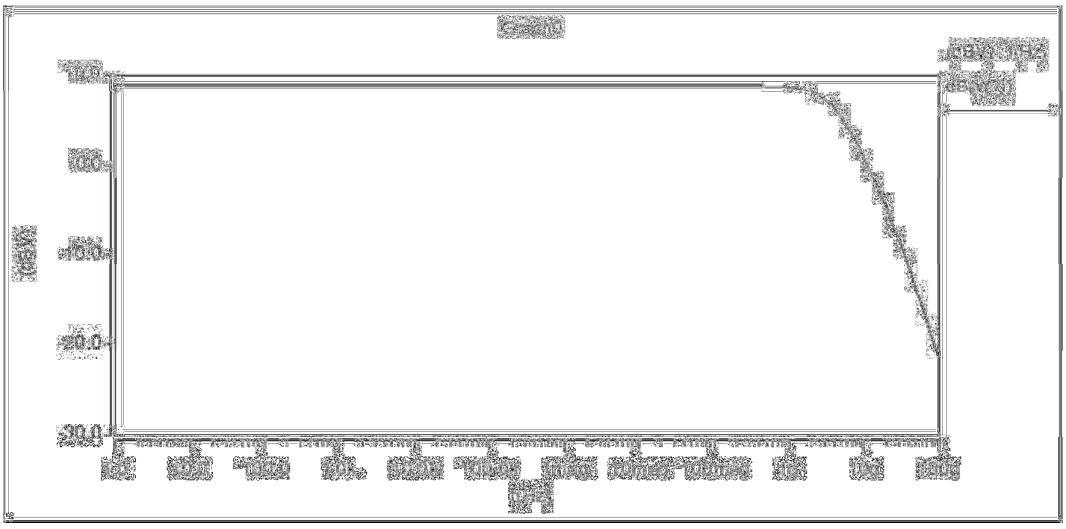


Fig 4.5 Frequency response of CMOS Source Degeneration Differential Amplifier

Phase Response Curve of CMOS Source Degeneration Differential Amplifier shows phase margin of 104.8°.

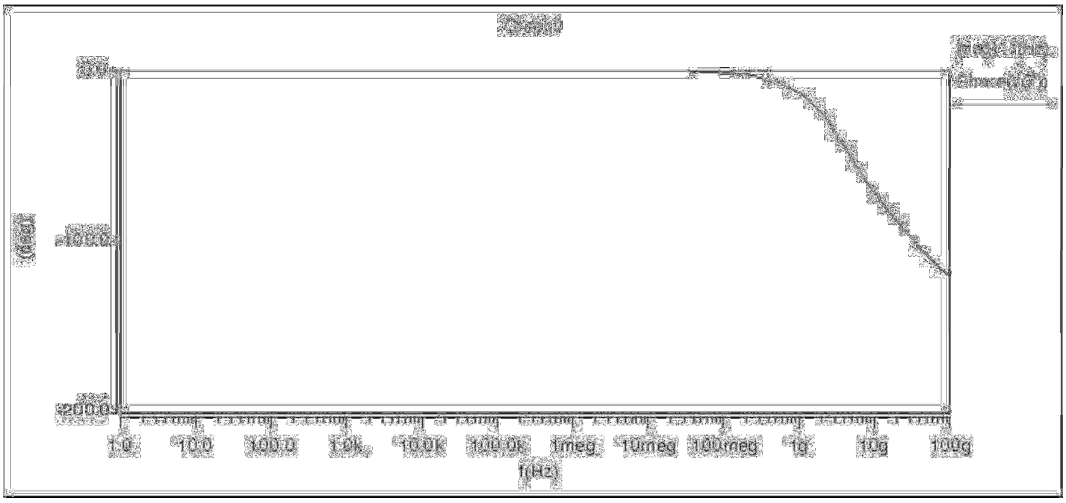


Fig 4.6 Phase Curve of CMOS Source Degeneration Differential Amplifier

4.3 Multiple Signal Differential Amplifier:

Transfer Curve between input and output voltage shows linearity between range -0.5V to +0.5V where amplifier can work properly

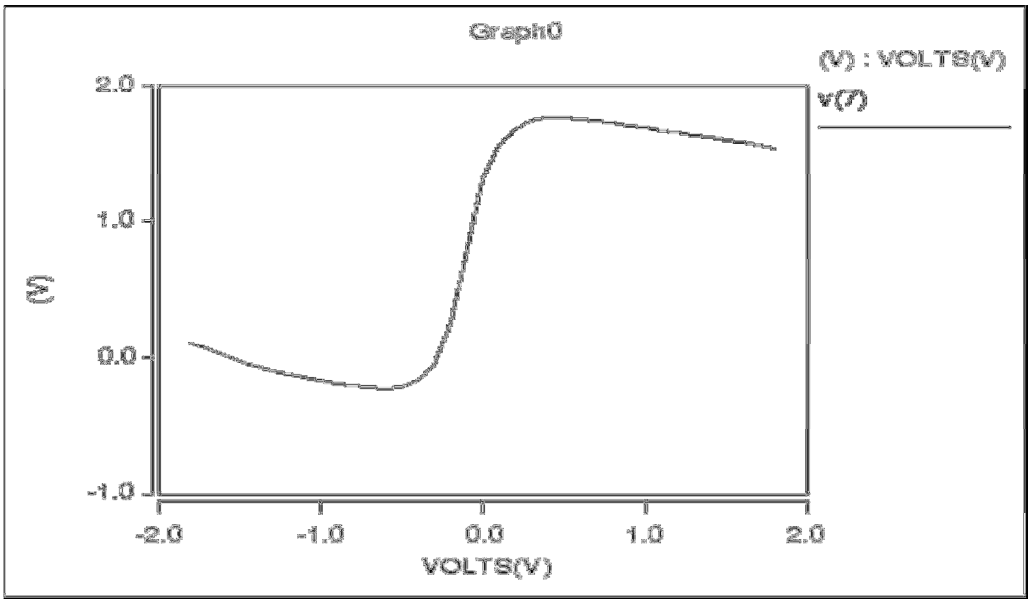


Fig 4.7 Transfer Curve of CMOS Multiple Signal Differential Amplifier

The Bandwidth of Source Degeneration is 17 Ghz and gain is 11.85 db as seen from frequency response curve.

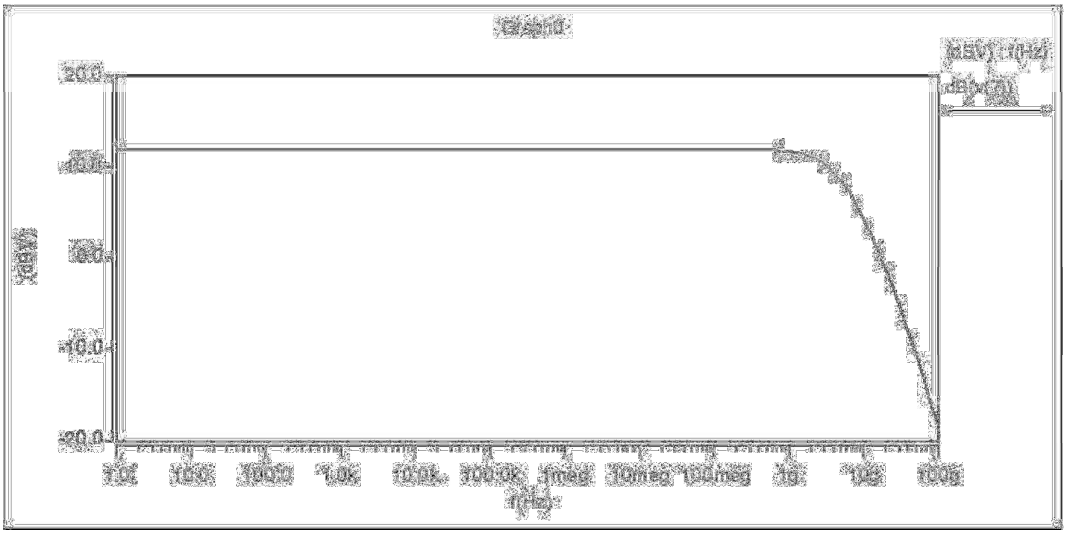


Fig 4.8 Frequency response of CMOS Multiple Signal Differential Amplifier

CMOS Multiple Signal Differential Amplifier provides phase margin of 95°

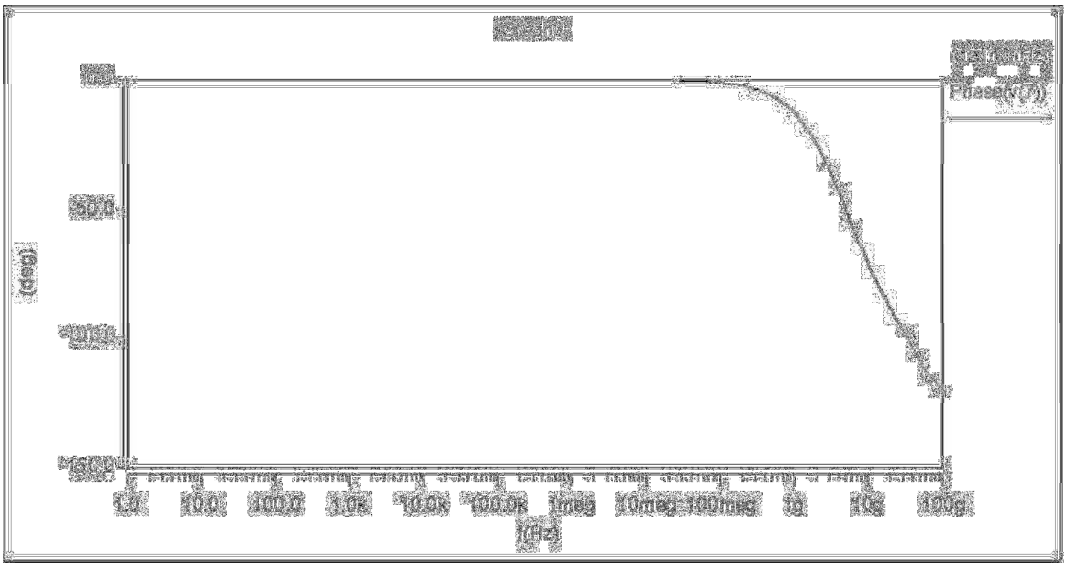


Fig 4.9 Phase Curve of CMOS Multiple Signal Differential Amplifier

4.3 CMOS Resistive Common mode differential Amplifier:

Transfer Characteristics of CMOS Resistive Common mode differential amplifier is in linear region for values ranging -0.5V to +0.5V

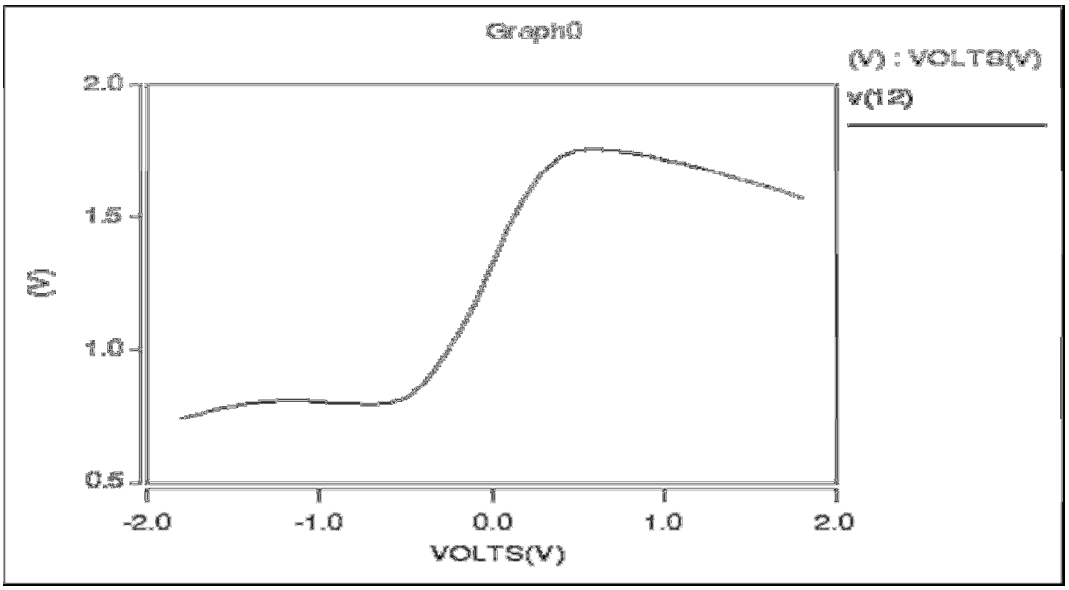


Fig 4.10 Transfer Curve of CMOS Resistive Common mode differential Amplifier

Frequency response curve of CMOS resistive common mode provides a bandwidth of 7.59 Ghz and gain of 3.58 db

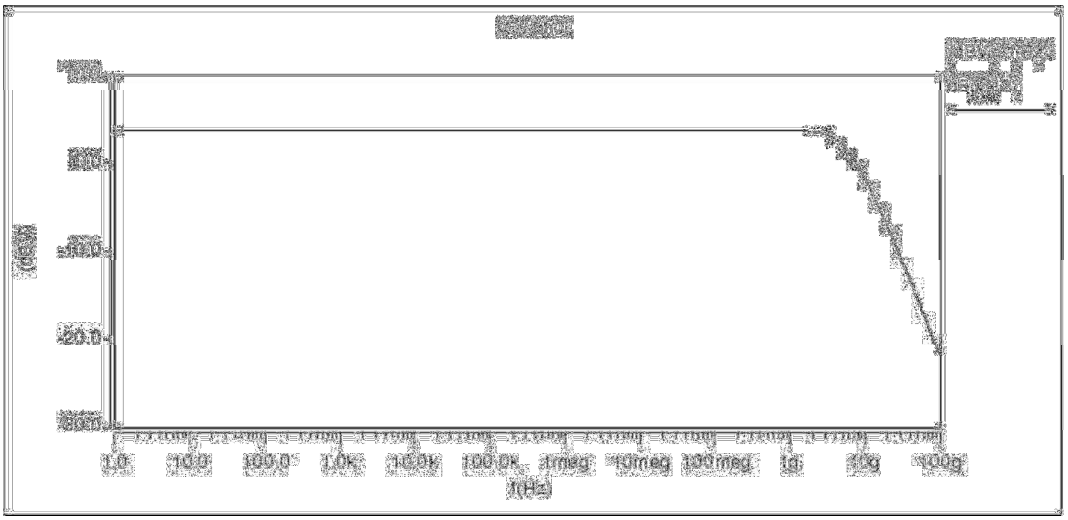


Fig 4.11 Frequency response curve of CMOS Resistive Common mode Differential Amplifier

Phase Margin of CMOS Resistive Common mode is 124˚ which is higher than other topologies of differential amplifier

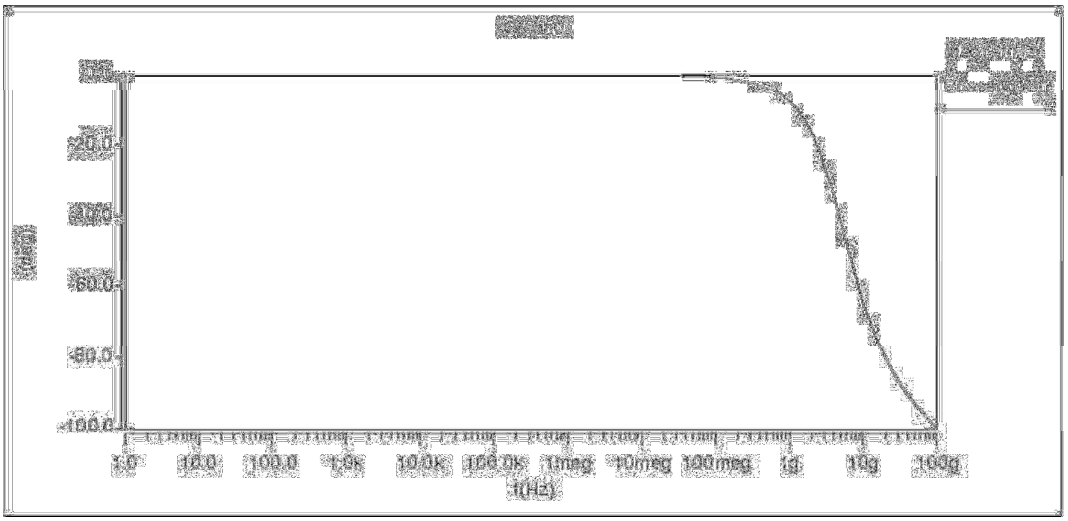


Fig 4.12 Phase Curve of CMOS Resistive Common mode Differential Amplifier

4.5 CMOS Resistive Cross coupled common mode feedback Differential Amplifier

Transfer Curve of CMOS Resistive Cross coupled common mode feedback differential amplifier shows very small region of operation of around 0.2 range which makes it less desirable

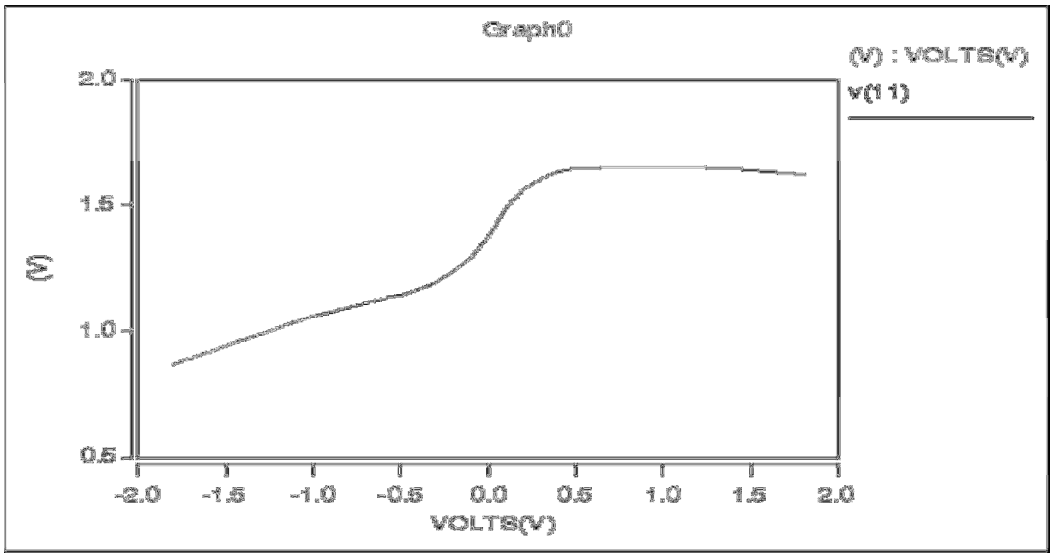


Fig 4.13 Transfer Curve of CMOS Resistive cross coupled common mode feedback differential amplifier

Frequency response of CMOS Resistive cross coupled common mode feedback differential amplifier gives operating frequency range with bandwidth of 4.4 Ghz and Gain is 11.63 db

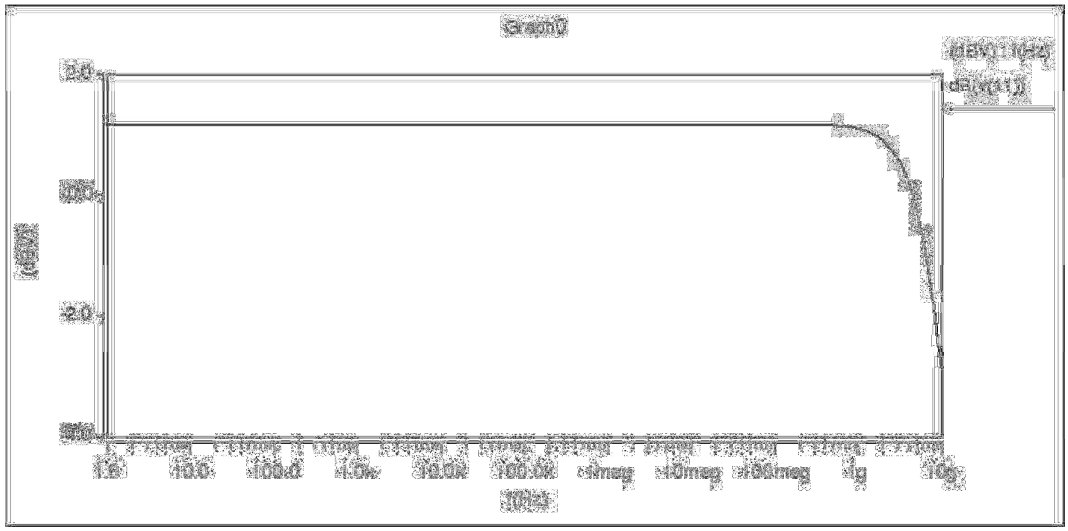


Fig 4.14 Frequency response Curve of CMOS Resistive cross coupled common mode feedback differential amplifier

Phase Curve of CMOS Resistive cross coupled differential amplifier provides phase margin of 149° which is highest

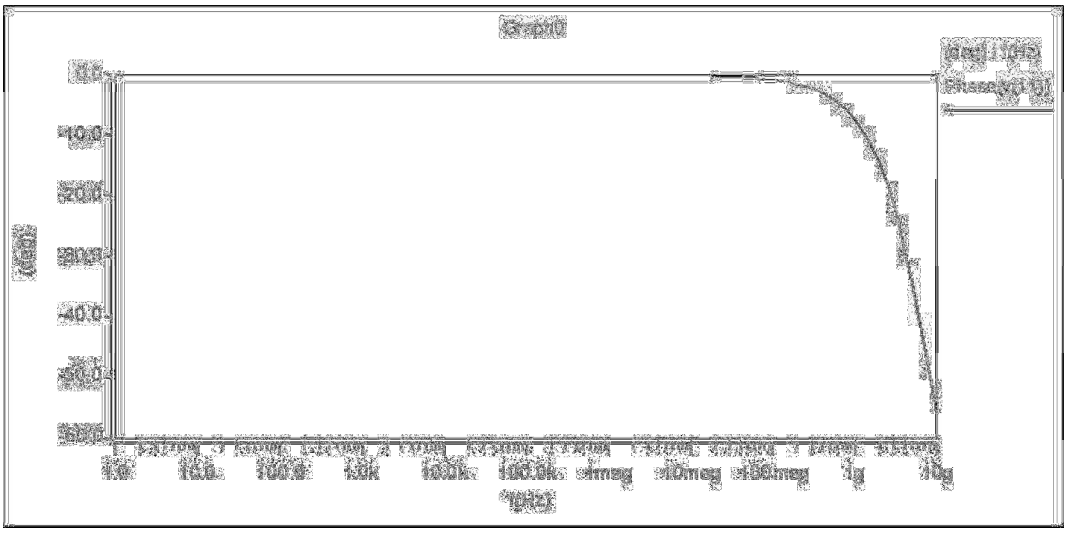


Fig 4.15 Phase Curve of CMOS Resistive cross coupled common mode feedback differential amplifier

4.6 CMOS Positive Feedback Differential Amplifier:

Transfer Curve of CMOS Positive Feedback Differential Amplifier shows linearity from -0.2V to +0.2V of input voltage range

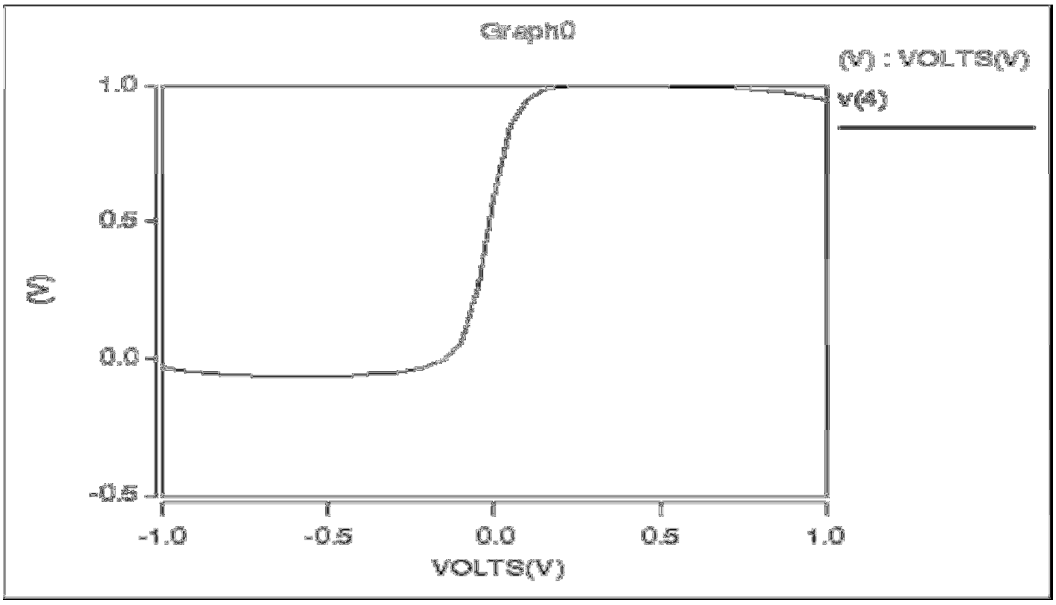


Fig 4.16 Transfer Curve of CMOS Positive Feedback Differential Amplifier

Frequency Response shows very high bandwidth of 28.4Ghz and give high Gain of 16.4 db

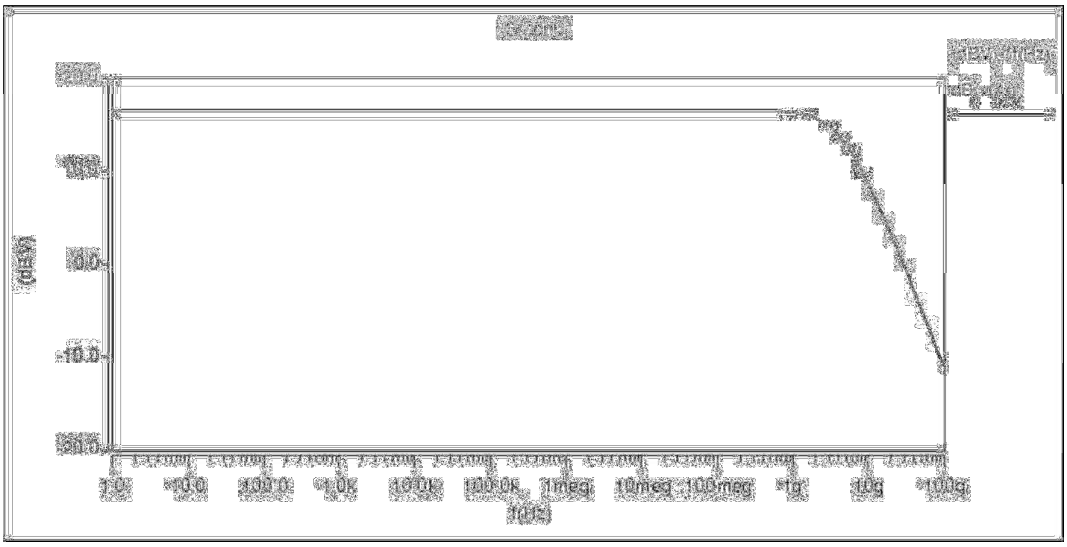


Fig 4.17 Frequency response curve of CMOS Positive feedback differential amplifier

Phase Margin of CMOS Positive Feedback Differential Amplifier is 91˚ which is lowest among different differential amplifiers

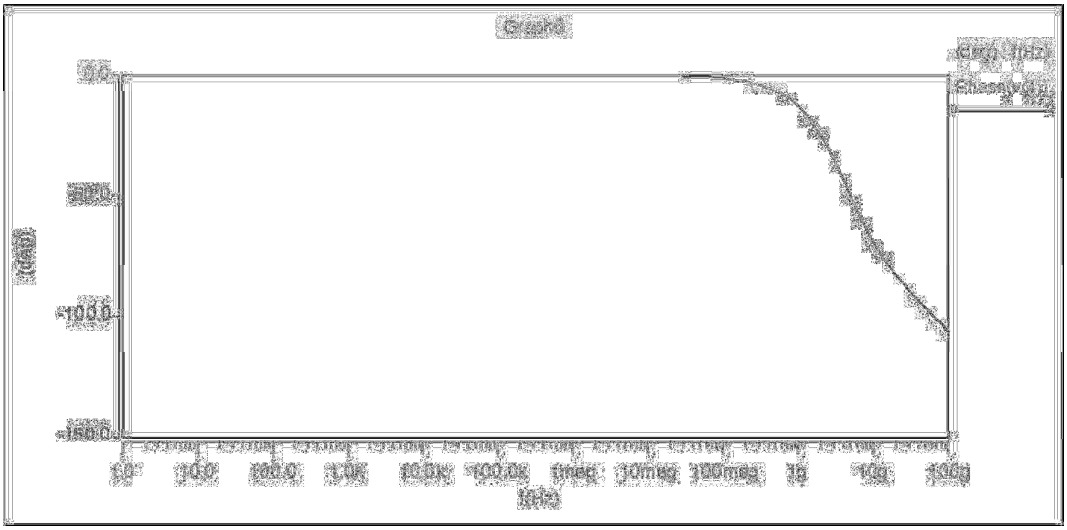


Fig 4.18 Phase Curve of CMOS Positive Feedback Differential Amplifier

4.7 CMOS Cascoded Differential Amplifier

Transfer curve gives region of operation of differential amplifier which can be seen as linear region where both transistors are saturated

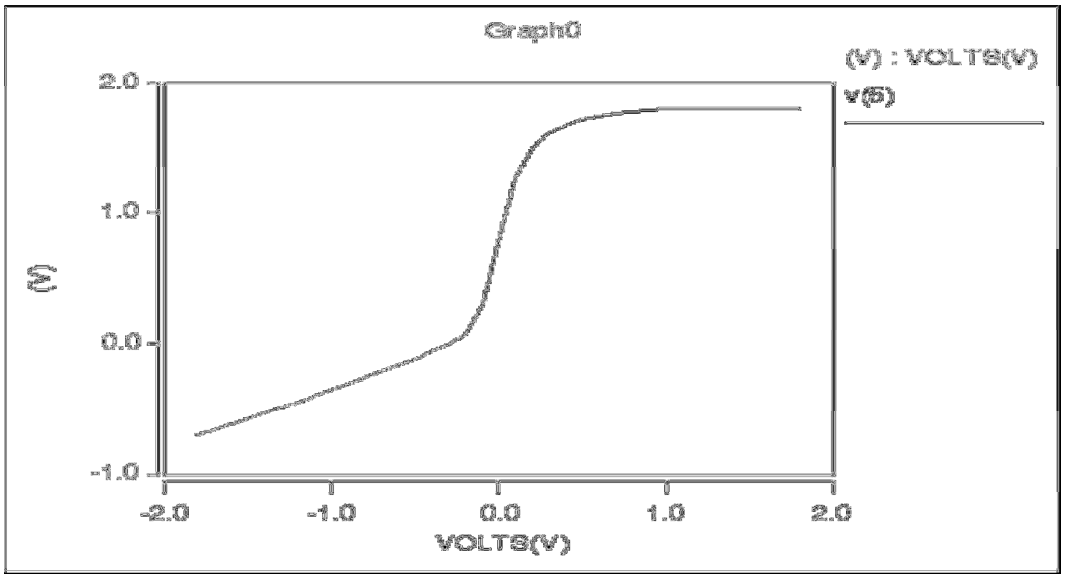


Fig 4.19 Transfer Curve of CMOS Cascoded Differential Amplifier

Frequency Response Curve of Cascoded differential amplifier provides low bandwidth of 4.6 Ghz and Gain of 14.4 db

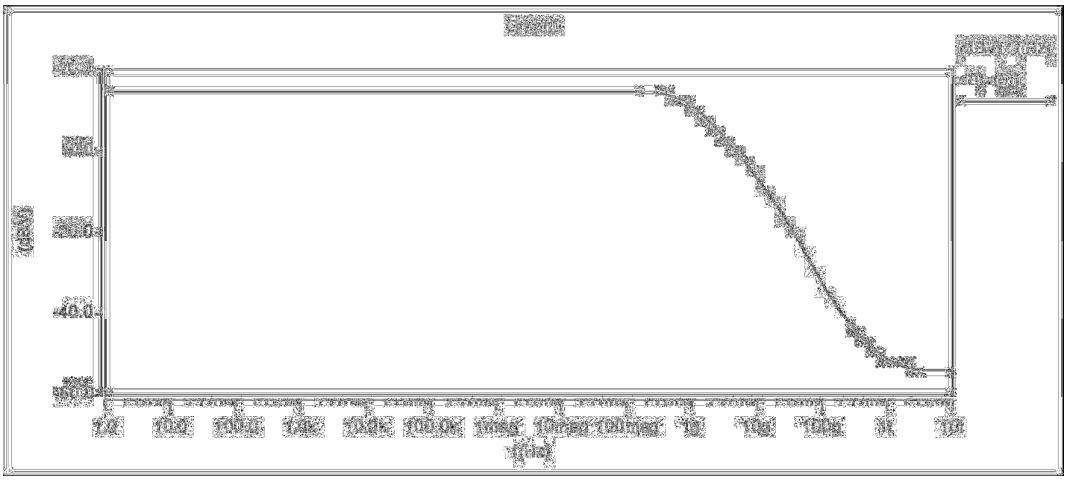


Fig 4.20 Frequency response curve of CMOS Cascoded Differential Amplifier

Phase Curve of CMOS cascaded differential amplifier gives phase margin of 94.6°

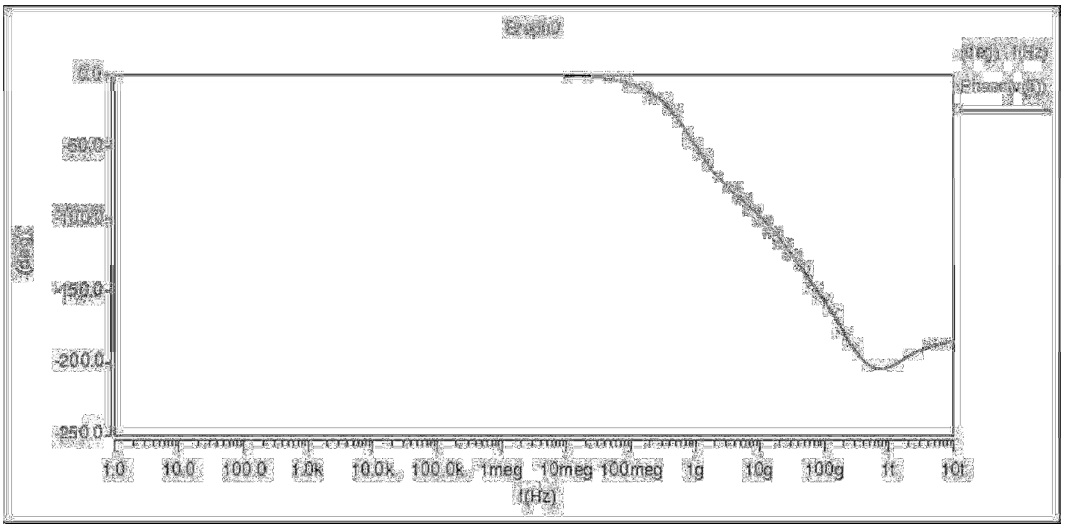


Fig 4.21 Phase Curve of CMOS Cascoded Differential Amplifier

Table 4.2 CNTFET Differential Amplifiers

	Differential amplifier with active load	Source degeneration differential amplifier	Multiple signal differential amplifier	Resistive common mode differential amplifier	Resistive cross coupled common mode feedback	Positive feedback Differential amplifier	Cascode Differential amplifier
Power dissipation (mW)	164	219	219.6	219.6	219.6	186.7	109.8
Gain	15.3	10.6	13.2	10.8	17.8	22.58	19.3
Bandwidth (Ghz)	0.2	19.4	25	10.15	9.9	28.3	1.4
Phase Margin	99.75	106.15	102.2	106	96.7	92.1	95.26
CMRR	33	35	36.8	49.6	57	52.99	44.6

4.8 CNT Differential Amplifier with Active Load:

Transfer characteristics of CNT differential amplifier with active load is linear in the range from -0.1V to +0.1V and in saturation region for other values of input voltage for given supply voltage.

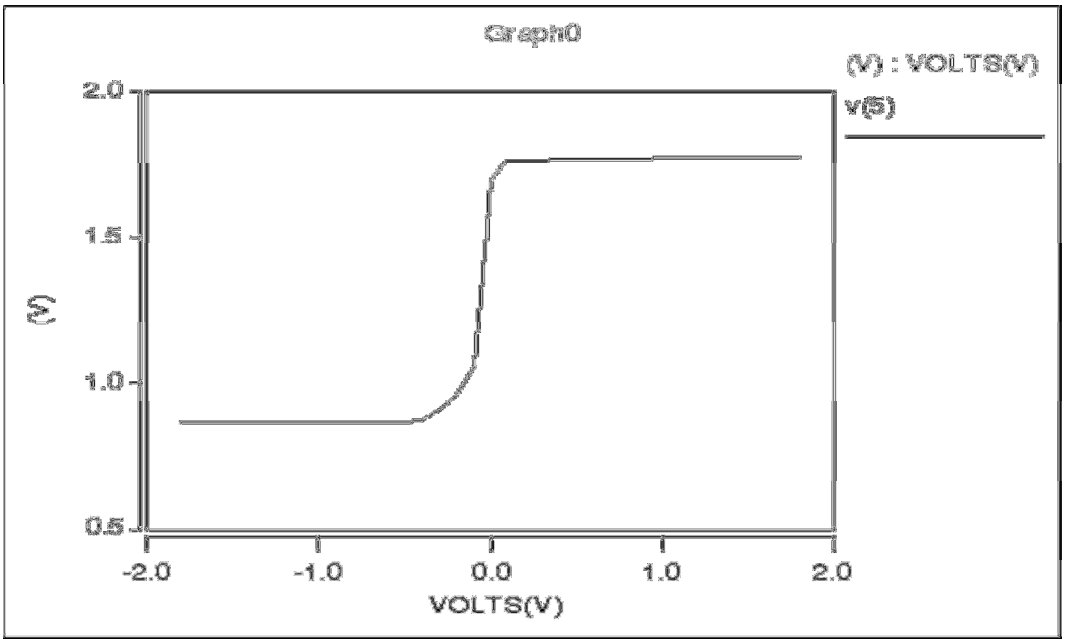


Fig 4.22 Transfer curve of CNT Differential Amplifier with Active Load

Frequency Response Curve of CNT differential Amplifier with active load is plotted between output voltage on y-axis and frequencies on x-axis provides bandwidth of 0.2Mhz and gain of 15.3 db

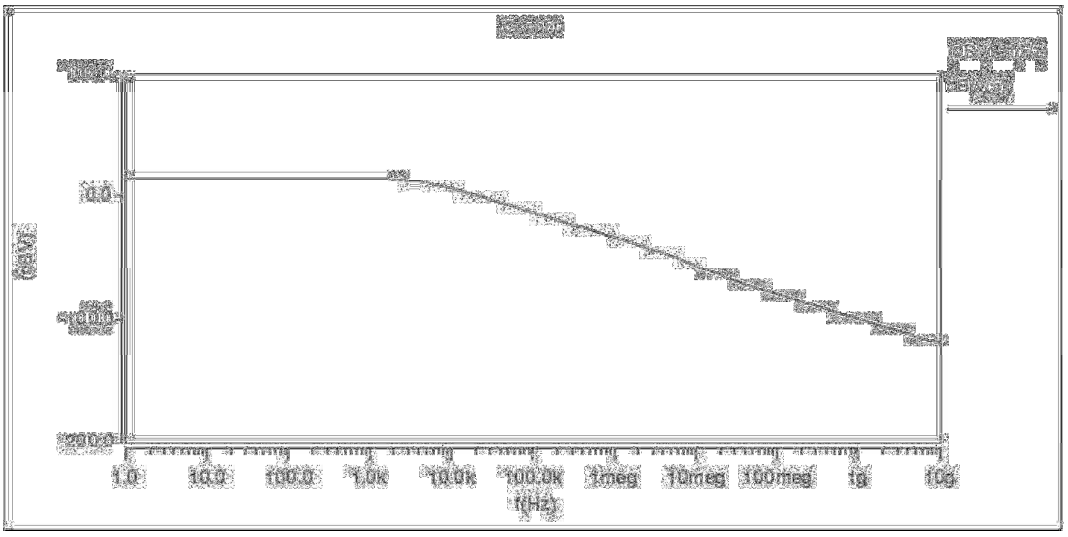


Fig 4.23 Frequency response curve of CNT Differential Amplifier with Active Load

Phase curve of CNT differential Amplifier with active load is plotted between phase and frequencies on Y and X axis respectively .It gives phase margin of 99.75°

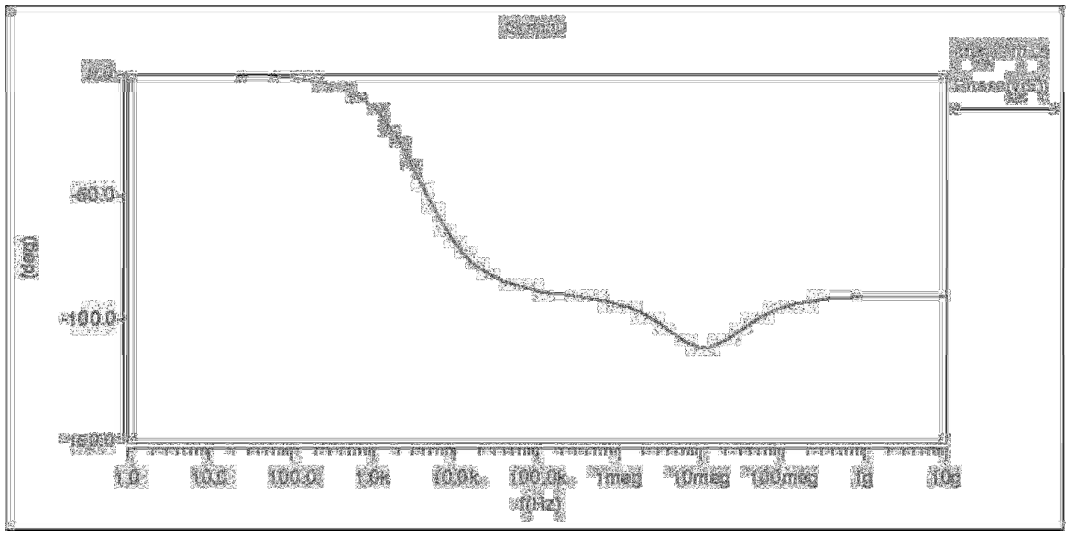


Fig 4.24 Phase curve of CNT Differential Amplifier with Active Load

4.9 CNT Source Degeneration Differential Amplifier:

Transfer Characteristics of CNT Source Degeneration Differential Amplifier shows that amplifier operates in linear region for values -0.2V to +0.2V and for values above or below this range either of the mosfet enter into non saturation

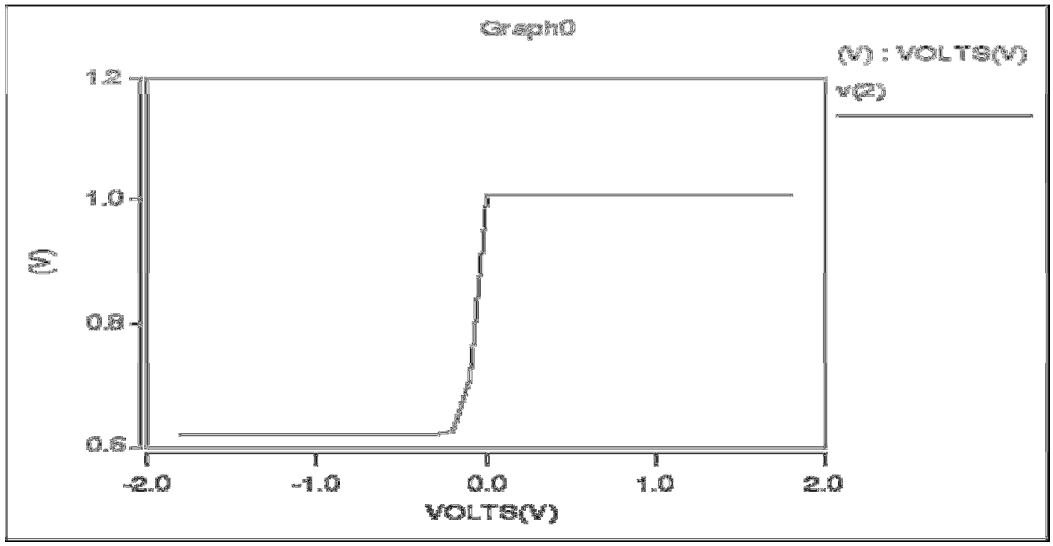


Fig 4.25 Transfer curve of CNT Source Degeneration Differential Amplifier

The frequency response is a plot between output voltage and different frequencies. Bandwidth of Source Degeneration is 19.4 Ghz and gain is 10.6 db as seen from frequency response curve.

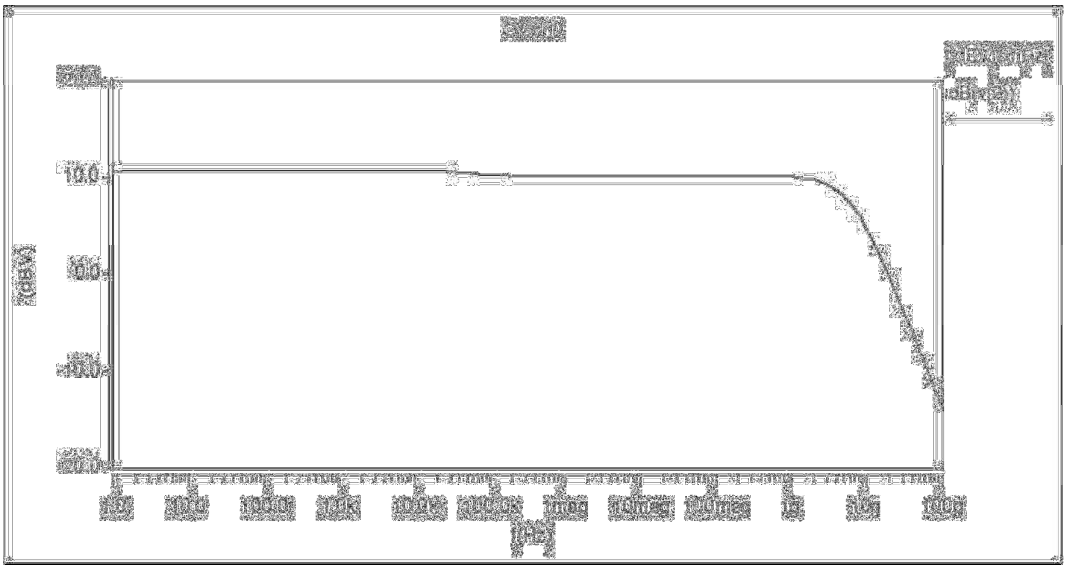


Fig 4.26 Frequency response curve of CNT Source Degeneration Differential Amplifier

Phase Response Curve of CNT Source Degeneration Differential Amplifier consist of phases on Y axis and frequencies on the X axis . Graph shows phase margin of 106.15°

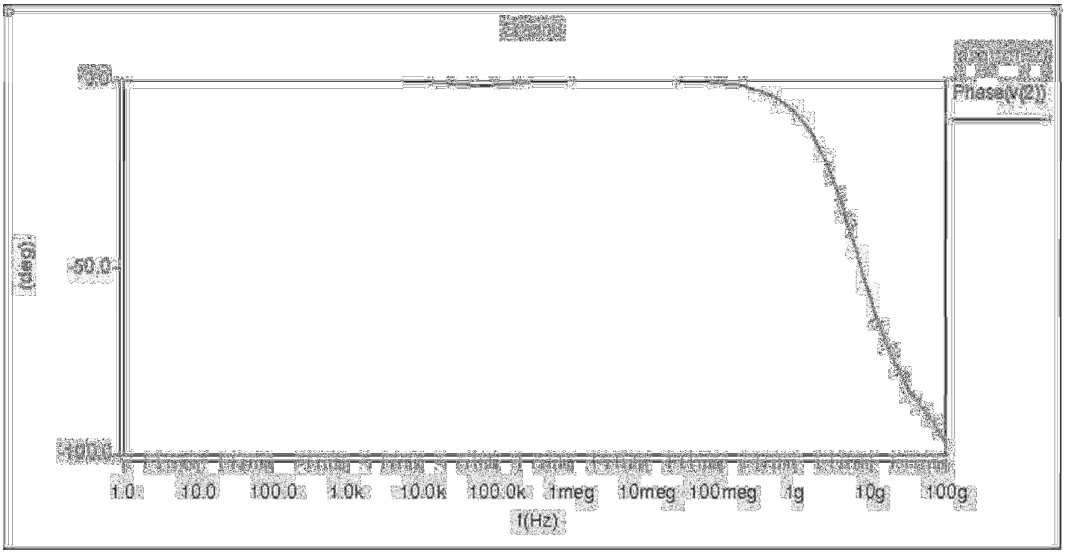


Fig 4.27 Phase curve of CNT Source Degeneration Differential Amplifier

4.10 CNT Multiple Signal Differential Amplifier:

Transfer Curve between input and output voltage shows linearity between range -0.2V to +0.2V where amplifier can work properly

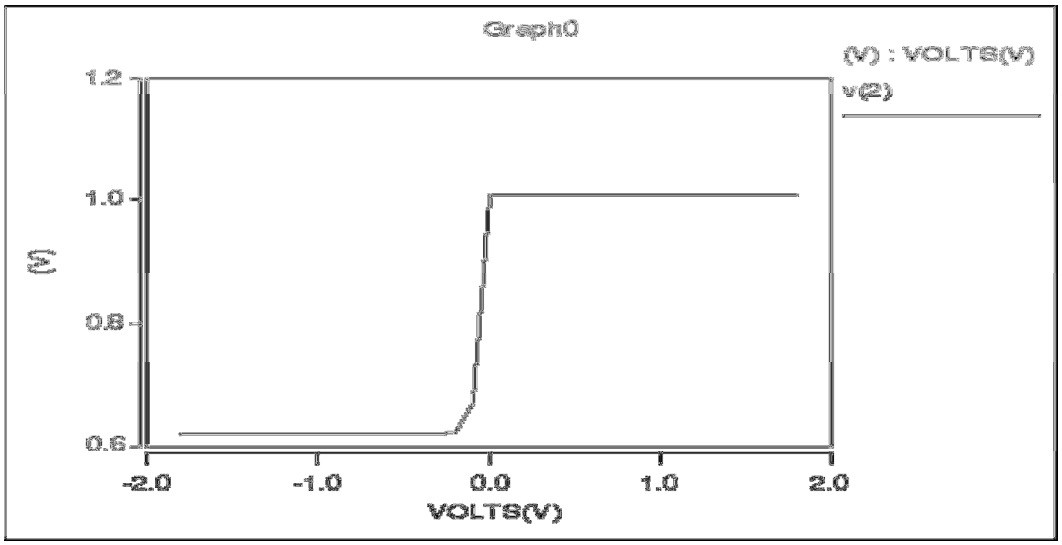


Fig 4.28 Transfer curve ofCNT Multiple Signal Differential Amplifier

The frequency response curve gives range of frequencies upto which gain is constant .Bandwidth of CNT Source Degeneration is 25 Ghz and gain is 13.2 db.

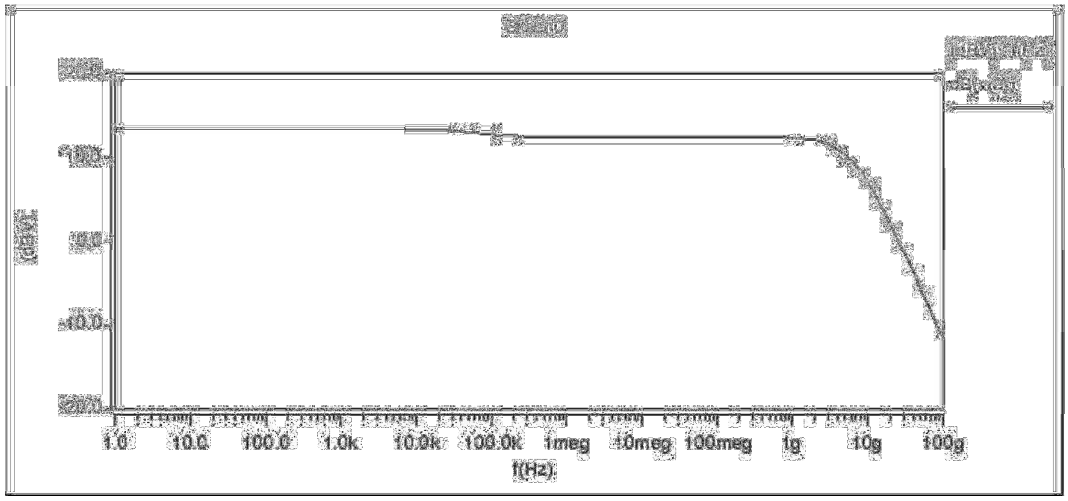


Fig 4.29 Frequency response curve ofCNT Multiple Signal Differential Amplifier

CNT Multiple Signal Differential Amplifier phase curve gives the value of phase which when added can drag the circuit on verge of unstability and that value for given curve is 102.2°

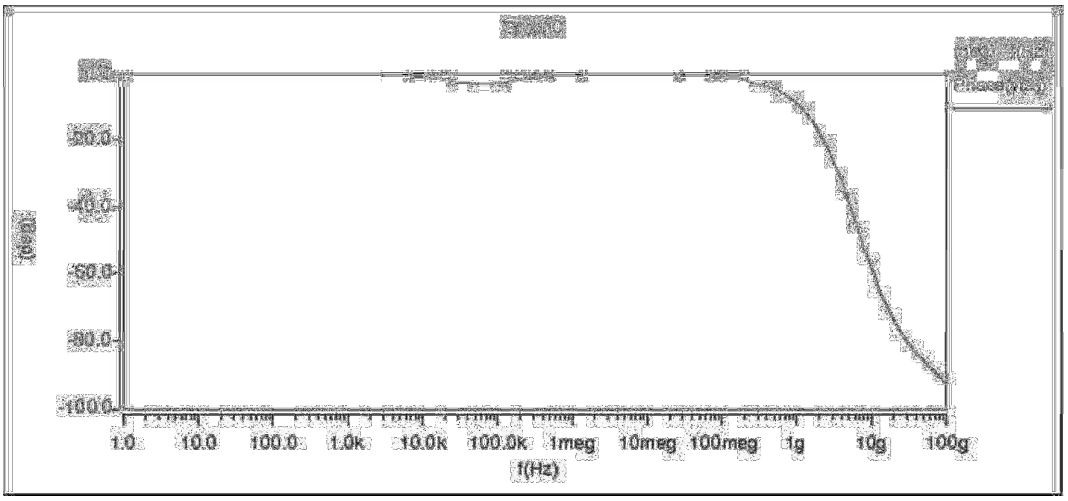


Fig 4.30 Phase curve ofCNT Multiple Signal Differential Amplifier

4.11 CNT Resistive Commmon mode Differential Amplifier:

Transfer Characteristics of CNT Resistive Common mode differential amplifier gives linear region of operation for the differential amplifier whose values ranges from -0.2V to +0.2V

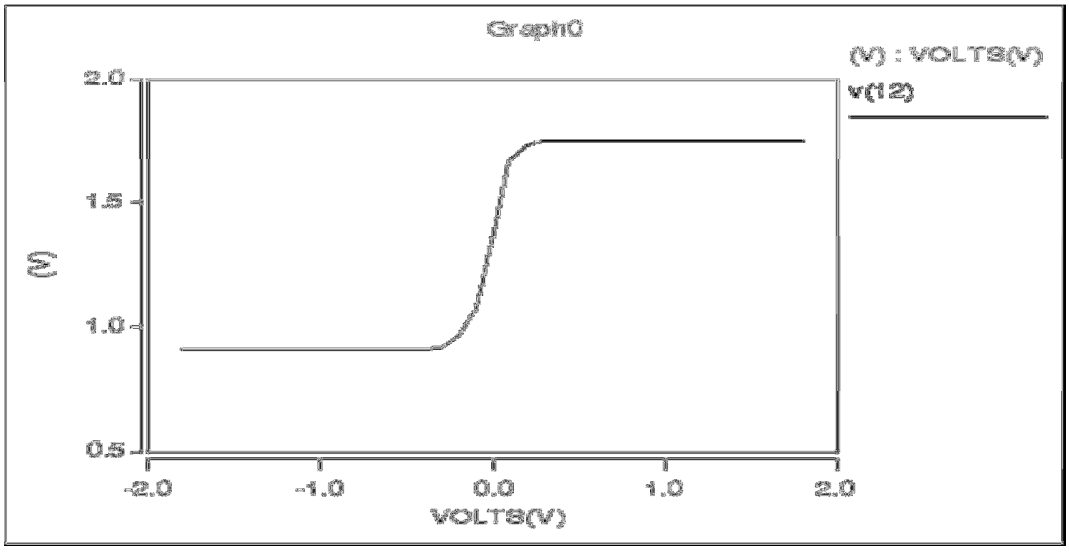


Fig 4.31 Transfer curve of CNT Resistive Commmon mode Differential Amplifier

Frequency response curve of CNT resistive common mode provides the bandwidth for which gain is constant, and bandwidth and gain of CNT common mode is 10.15 Ghz and of 10.8 db respectively

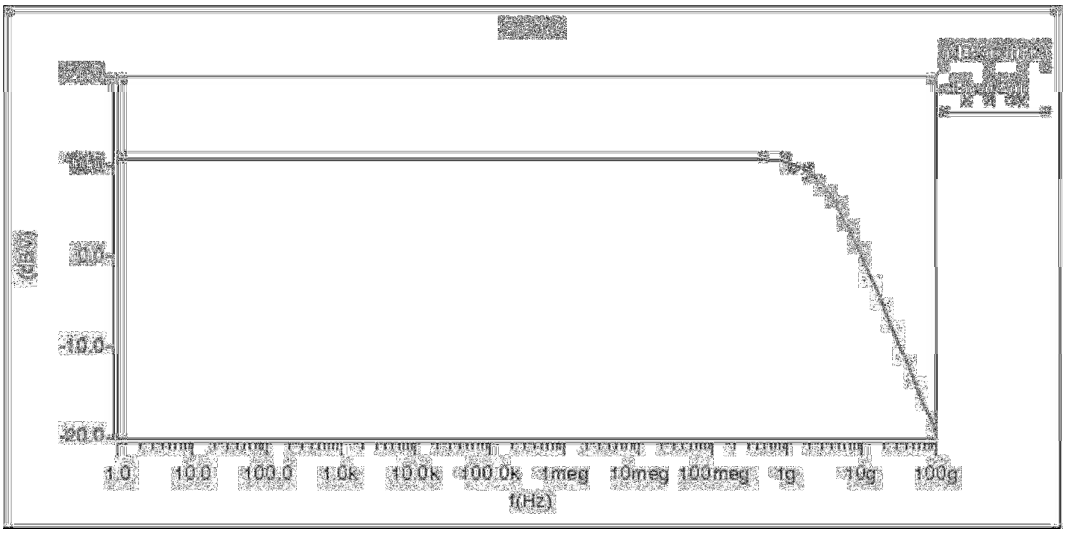


Fig 4.32 Frequency response curve of CNT Resistive Common mode Differential Amplifier

Phase Margin of CNT Resistive Common mode is 106˚ which is higher than other topologies of differential amplifier

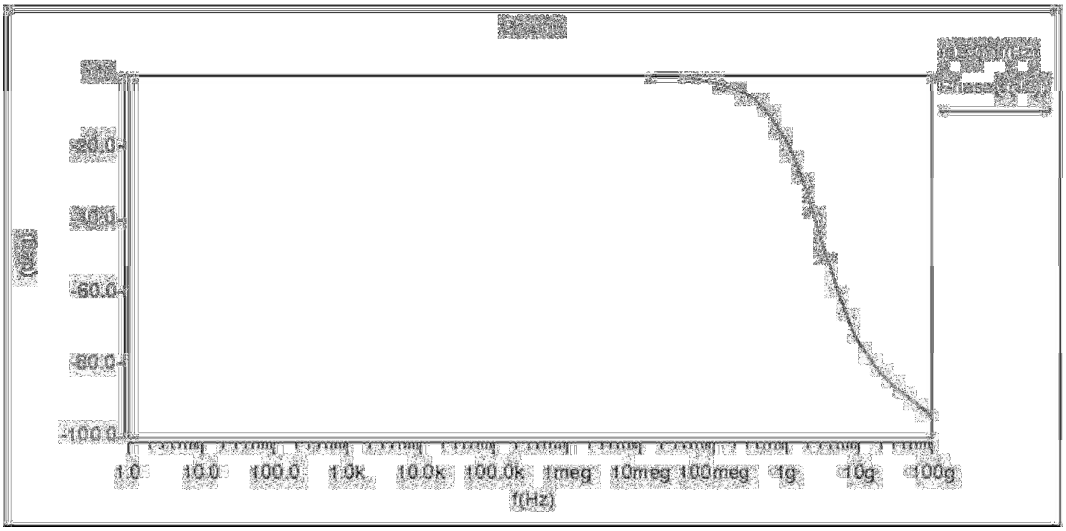


Fig 4.33 Phase curve of CNT Resistive Common mode Differential Amplifier

4.12 CNTFET Resistive Cross coupled common mode differential Amplifier:

Transfer Curve of CNT Resistive Cross coupled common mode feedback differential amplifier shows v region of operation of around 0.4 range which makes it less desirable

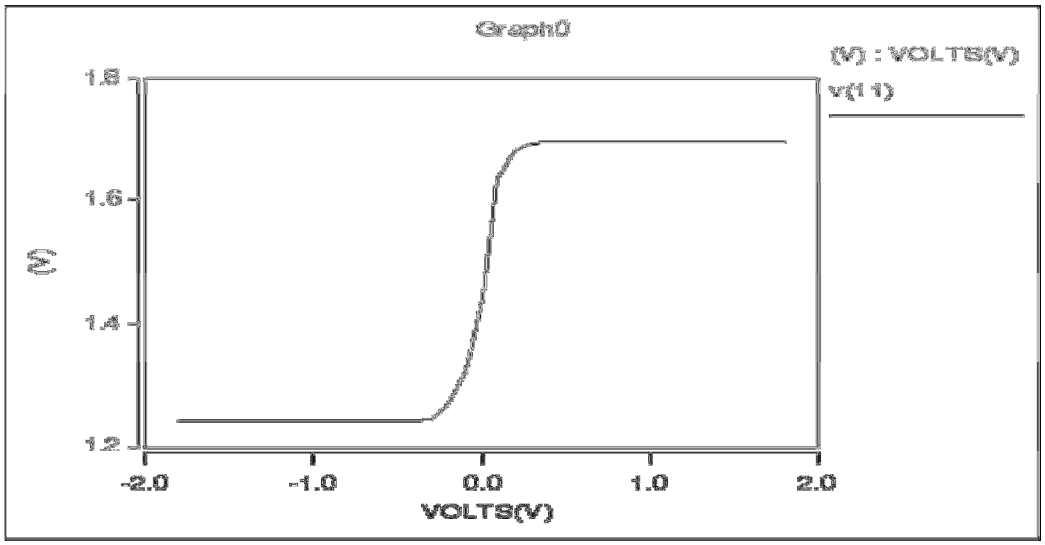


Fig 4.34 Transfer curve of CNTFET Resistive Cross coupled common mode differential Amplifier

Frequency response of CNT Resistive cross coupled common mode feedback differential amplifier gives operating frequency range with bandwidth of 9.9 Ghz and Gain is 17.8 db

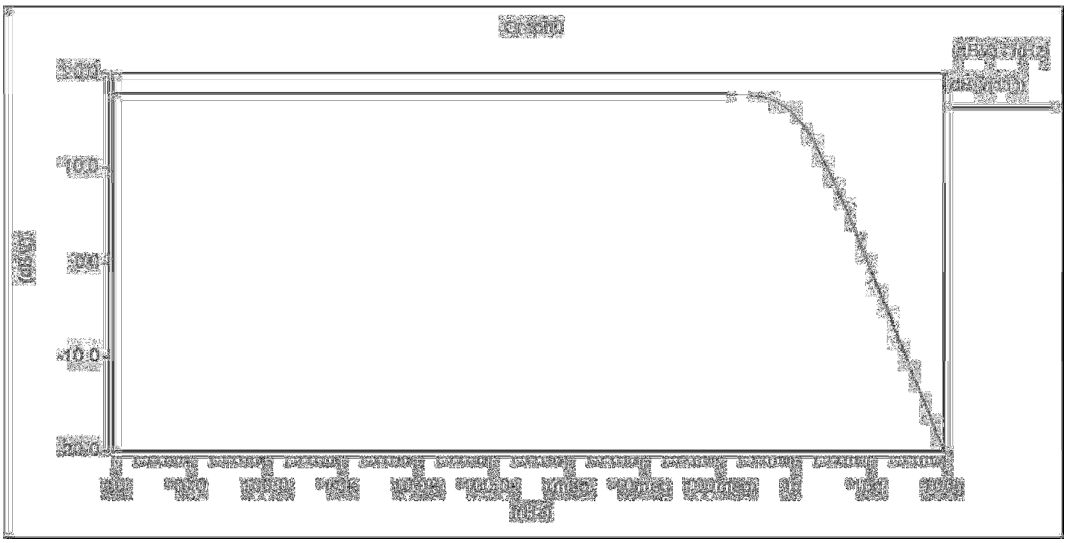


Fig 4.35 Frequency response curve of CNTFET Resistive Cross coupled common mode differential Amplifier

Phase Curve of CNT Resistive cross coupled differential amplifier provides phase margin of 96.7°

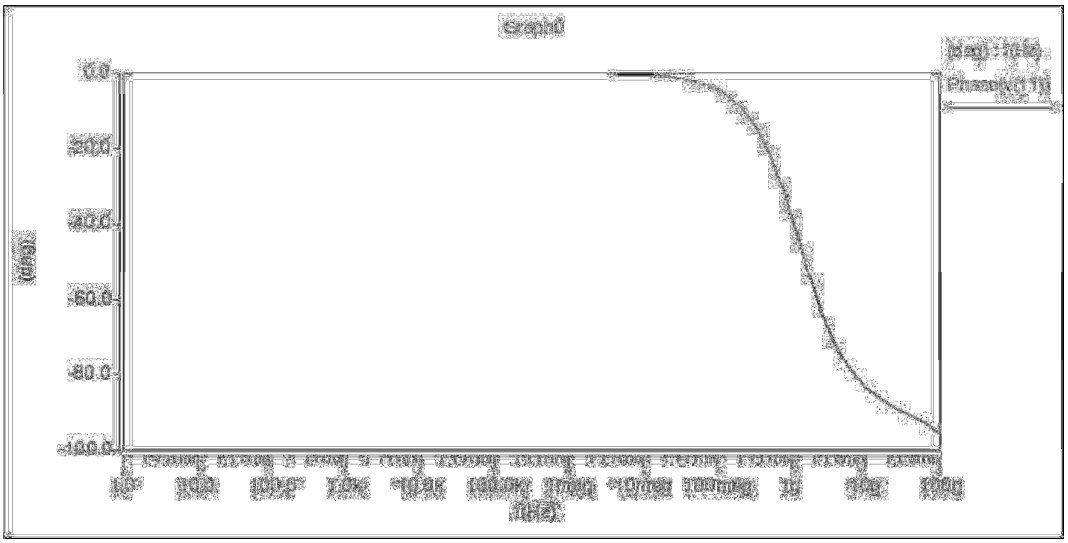


Fig 4.36 Phase curve CNTFET Resistive Cross coupled common mode differential Amplifier

4.13 CNTFET Positive Feedback Differential Amplifier:

Transfer Curve of CNT Positive Feedback Differential Amplifier shows linearity from -0.2V to +0.2V of input voltage range

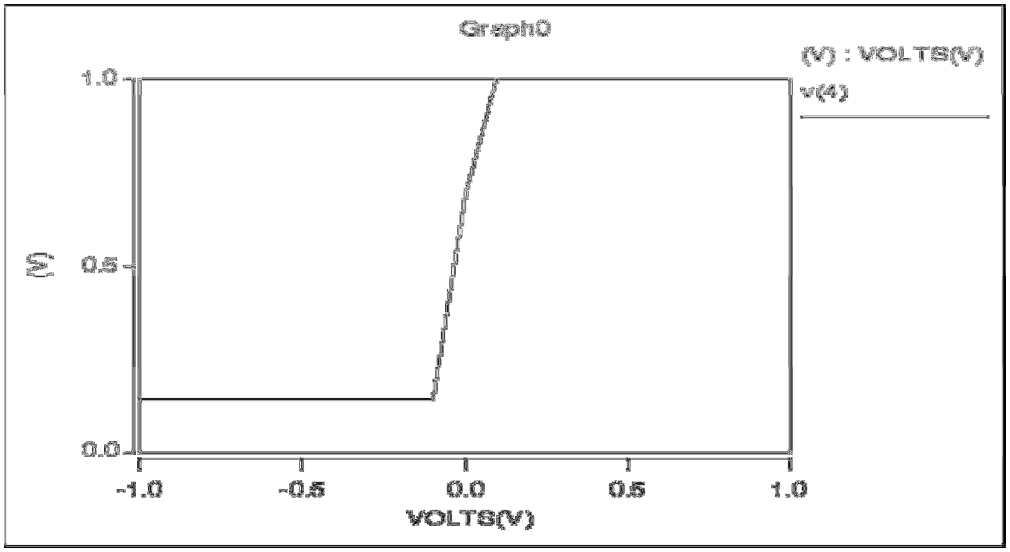


Fig 4.37 Transfer curve of CNTFET Positive Feedback Differential Amplifier

Frequency Response shows very high bandwidth of 28.3 Ghz and give high Gain of 22.58 db.

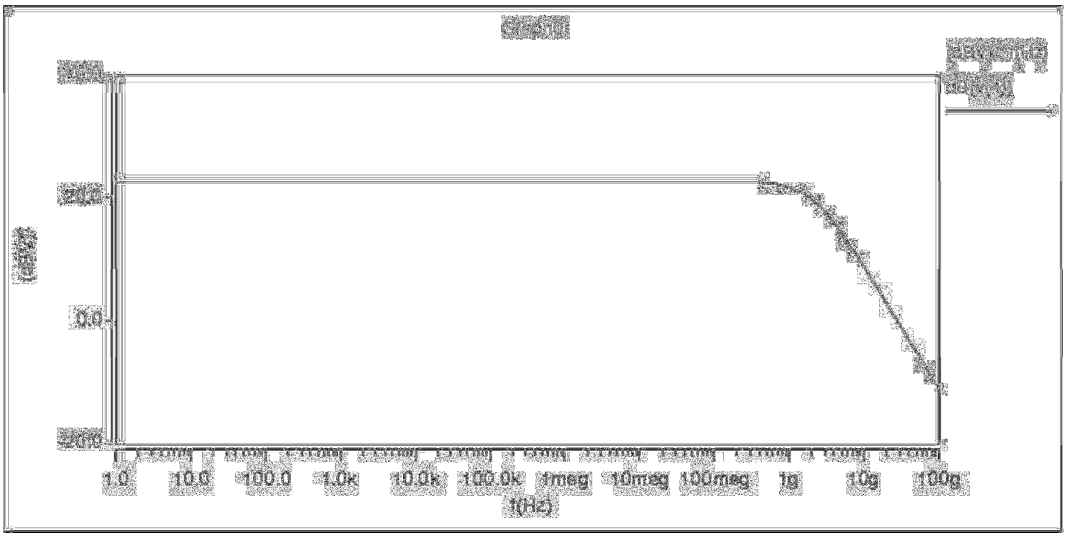


Fig 4.38 Frequency response curve of CNTFET Positive Feedback Differential Amplifier

Phase Margin of CNT Positive Feedback Differential Amplifier is 92.1˚

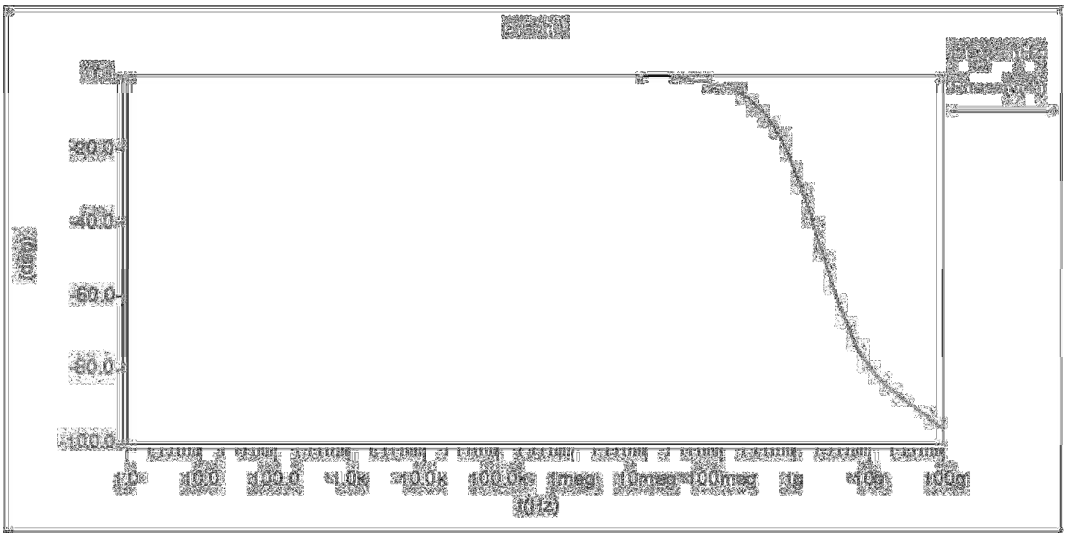


Fig 4.39 Phase curve of CNTFET Positive Feedback Differential Amplifier

4.14 CNTFET Cascoded Differential Amplifier:

Transfer curve gives region of operation of differential amplifier which can be seen as linear region where both transistors are saturated

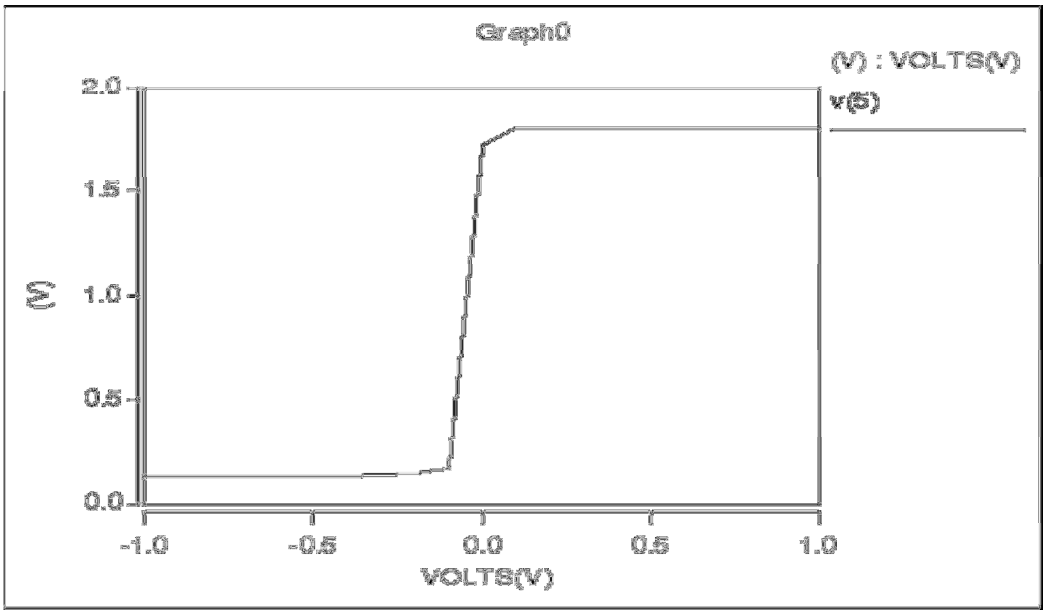


Fig 4.40 Transfer curve of CNTFET Cascoded Differential Amplifier

Frequency Response Curve of Cascoded differential amplifier provides low bandwidth of 1.4 Ghz and Gain of 19.3 db

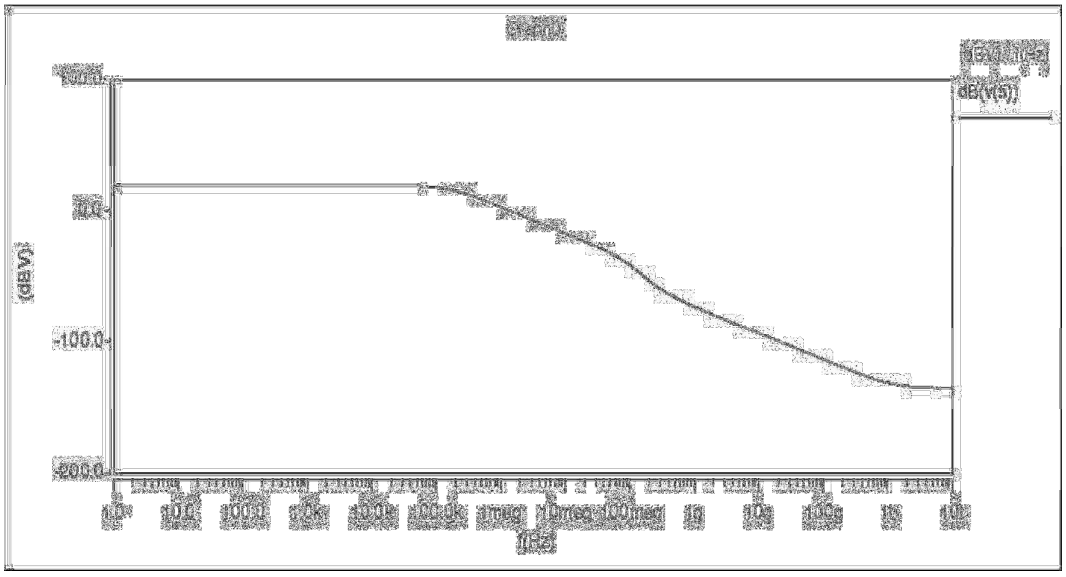


Fig 4.41 Frequency response curve of CNTFET Cascoded Differential Amplifier

Phase Curve of CNT cascaded differential amplifier gives phase margin of 95.26°

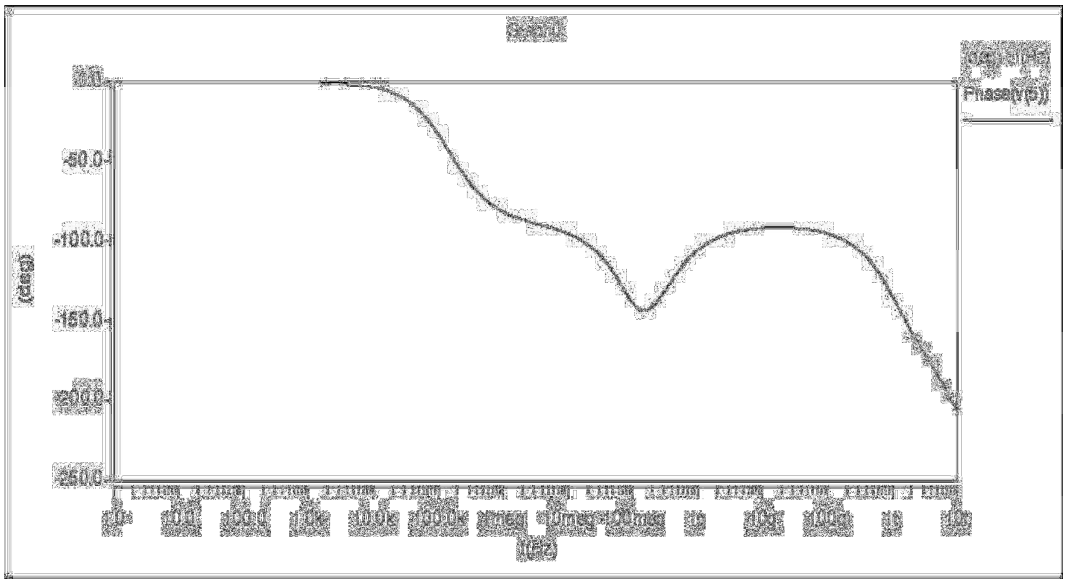


Fig 4.42 Phase curve of CNTFET Cascoded Differential Amplifier

It can be clearly seen from above transfer and frequency response curves of various differential amplifier, gain of CMOS positive feedback differential amplifier is highest moreover bandwidth is comparatively high. When CMOS is replaced by CNTFET the characteristics get further improved, thus making the differential amplifier application to more complex circuits which require high gain for better signal amplification.

Positive feedback differential amplifier shows low phase margin when compared to other topologies of differential amplifier but advantages of high gain and bandwidth makes positive feedback differential amplifier desirable for many analog circuits.

Summary and Conclusions

Chapter 5 SUMMARY AND CONCLUSION

This thesis work studies the change in parameters value of different topologies of Differential amplifier in CMOS and in CNTFET. First of all different circuits of differential amplifiers are simulated in CMOS technology for 32nm and same has been simulated in CNTFET technology.

Various parameters like Power Dissipation, Gain, CMRR, Phase Margin and Bandwidth has been measured for CMOS and CNTFET and resultant graphs have been plotted to indicate the variation of one circuit from another with the help of transfer curve, frequency and phase response curves. When compared different circuits in CMOS, Positive Feedback Differential Amplifier provided higher Gain and Bandwidth which are the deciding factors for designing of differential amplifier. A good differential amplifier is expected to give high gain, bandwidth with minimum power dissipation. But in CMOS with scaling down, performance of circuit deteriotes whereas CNTFET are specifically designed to work at nanoscale. CNTFET are defined by their indices m and n which determine its diameter and chirality. The diameter can be changed which changes the properties of the device.

When different Differential circuits are simulated in 32nm technology using CMOS as well as in CNTFET, results are better for CNTFET technology .Among various circuits which are analysed using HSPICE, Positive Feedback Differential Amplifier has shown higher values of parameters like Gain and Bandwidth and results get further improved for CNTFET based Positive Feedback Differential amplifier which can increase the efficiency of operational amplifier where it is used at initial stage.

Literature Cited

LITERATURE CITED

Apirak Suadet, Varakom Kasemsuwan (2010) "A CMOS inverter based class AB pseudo differential amplifier for HF applications" *IEEE International Conference of Electron Devices and Solid State Circuits 15-17 Dec 2010*

Arbet Daniel. Kovac Martin. Nagy Gabrial. Stopjakkova Viera (2015) "High dynamic range and low distortion fully differential difference amplifier in CMOS." *IEEE 25th International Conference Radioelectronica* 21-22April 2015

Baker R. Jacob "CMOS Circuit design, Layout and Simulation" *IEEE third edition.*

Behzad Razavi "Design of Analog CMOS Integrated Circuits" *University of California McGraw-Hill Higher Education, 2001 Edition*

Butkovic Z. and Szabo A. (2004) "Analysis of the CMOS differential amplifier with active load and single ended output" IEEE. *Proceedings of the 12th Mediterranean Electrotechnical Conference, MELECON 12-15 May 2004.*

Chen Hong. Milovanovic Vladimir. Giotta Dario. Zimmermann Horst (2013) "Ultra high bandwidth fully differential three stage operational amplifiers in 40 nm digital CMOS".*IEEE. 16th International Symposium on Design and Diagnostics of Electronic Circuits and Systems 8-10 April 2013*

Cheng Hui-Wen. Yiming Li (2010) "A comparative study of dynamic characteristics on 16 nm gate planar CMOS and bulk FinFETs' differential amplifier". *IEEE International Conference on Enabling Science and Nanotechnology (ESciNano), 24 January 2011*

Cosmin Popa(2010). "Improved linearity CMOS differential amplifiers with applications in VLSI designs" *IEEE 9th International Symposium on Electronics and Telecommunications (ISETC), 11-12 Nov. 2010*

Deferm Noel. Reynaert Patrick (2010) "A 100 GHz transformer coupled fully differential amplifier in 90nm CMOS"*IEEE Symposium on Radio Frequency Integrated Circuits 23-25 May 2010*

E. Sackinger, W. Guggerbuhl (1987) "A versatile building block CMOS differential difference amplifier" *IEEE. Journal of Solid State Circuits, VOL SC-22,No 2, April 1987*

Fahad Ali Usmani, Mohammad Hasan (2010) "Carbon nanotube field effect transistors for high performance analog applications: an optimum design approach"*IEEE Microelectronics Journal, Vol 41, Issue 7, July 2010*

Gianluca Giustolisi, Alfio Dario Grasso,Salvatore Pennisi (2007) "High Drive and Linear CMOS class AB Pseudo Differential Amplifier" *IEEE. Transactions on Circuits and Systems, VOL 54,No 2, February 2007*

Gomz H. Espinosa G (2014) "55 db DC gain, robust to PVT single stage fully differential amplifieron 45 nm SOI-CMOS technology" *Electronics letters Volume 50 Issue: 10, May 8 2014*

Grasso Alfio Dario. Monsurro Pietro. Pennisi Salvatore. Scotti Giuseppe. Trifiletti Alessandro (2009) "Analysis and Implementation of a minimum supply body biased CMOS Differential Amplifier Cell. *IEEE Transactions on very large scale Integration (VLSI) systems, VOL. 17, NO. 2, February 2009*

Hong Feng. R S David (2010) "Cumming Source compensation scheme for reducing impact of variability on differential amplifier in 35 nm CMOS."*IEEE* 17th *International Conference on Electronics, Circuits and Systems12-15 Dec. 2010*

K. Takenaka, K. Wada, S. Takagi, N. Fujii (2000) "Power saving technique for MOS differential amplifier" *IEEE International Symposium on Circuits and Systems 28-31 May 2000*

Li Chun-Hsing. Wei Chih. Nan Kuo Chien (2013) "A 147 GHz fully differential D-band amplifier design in 65 nm CMOS" *IEEE Asia Pacific Microwave Conference 5-8 Nov.*2013

Madiha Amina Protik Biswas. Aman Ullah.Iqbal Bahar Chowdhury(2015) "Analysis of common mode rejection ratio of a CMOS differential amplifier considering all the non idealities" *IEEE. International Conference on Electrical Information and Communication Technology 10-12 Dec 2015*

Mark Pude, P. R. Mukund, Prashant Singh, Ken Paradis, Jeff Burleson (2010) "Amplifier gain enhancement with positive feedback" *IEEE International Midwest Symposium on Circuit and Systems 1-4 Aug 2010*

Mattews T. W. (1997) "A CMOS differential amplifier with well controlled voltage gain." *IEEE. Proceedings of the 40th Midwest Symposium on Circuits and Systems, 6-6 Aug. 1997*

Mustafa Fayez, Khaled M.Morsi, M. Nabil Sabry (2016) "Design of OFET based differential amplifier with cascaded diode connected load" *IEEE International Conference on Microelectronics 17-20 Dec 2016 .*

Phillip E Allen . Douglas R Holberg (2002) "CMOS Analog Circuit Design" *New York Oxford University Press 2002*

Popa C. Coada D. (2003) "A new linearization technique for a CMOS differential amplifier using bulk driven weak inversion MOS transistors." *IEEE. International Symposium on Signals, Circuits and Systems SCS 10-11 July 2003*

Pulkin M. E. Connelly J. A. (1996). "A new CMOS differential amplifier circuit for Improved slew rate performance." *IEEE 39th Midwest symposium on Circuits and Systems 21-21 Aug. 1996*

S. Sedra Adel. C Smith Kenneth (2004) "Microelectronic Circuit" *New York Oxford University Press 2004 fifth edition*

Shenoy Aswin. Ajayan K R (2015) "Process variability on gain and bandwidth of a CMOS differential amplifier in 28 nm technology". *IEEE International Conference Control Communication& Computing India (ICCC), 14 March 2016*

Shinji Ohoka. Fumio Asakura. Hiroshi Taki (2015) "Electric field probe using a differential amplifier circuit with high input impedence" *IEEE Asia Pacific Symposium on Electromagnetic Compatilibity 26-29 May 2015*

Spiridon S. Eynde F (2005) "Low power CMOS fully differential variable gain amplifier" *IEEE Semiconductor Conference CAS 2005 Proceedings 3-5 Oct. 2005*

Thangarasu Bharatha Kumar, Kaixue Ma, Kiat Seng Yeo, Shouxian Mou, Mahalingam Nagarajan (2011) "A DC to 14GHz fully differential amplifier for wideband low power applications" *IEEE. International Design Conference 17-18 Nov 2011*

Thienen Niels Van. Reynaert Patrick (2014) "A 160-GHz three stage fully differential amplifier in 40nm CMOS."*IEEE. 21st IEEE International Conference on Electronic Circuits and System 7-10 Dec. 2014*

Vahdati Ali., Varonen Mikko. Parveg Dristy. Karaca Denizhen, Halonen A I Kari (2016) "Design of an 85-95 GHz differential amplifier in 28 nm CMOS FDSOI".*IEEE. Global Symposium on Millimeter Wave Technology 6-8 June 2016*

Visweswaran Akshay. Long R John. R Staszewki Bogdan (2014) "A 1.2V 110-MHz UGB differential class AB amplifier in 65nm CMOS"*IEEE. Proceedings of the Custom Integrated Circuits Conference (CICC) 15-17 Sept. 2014.*

Xiaojun Bi, Yongxin Guo, James Brinkhoff, Mook Seng Leong, Fujiang Lin (2010) "60 GHz unilteralized CMOS differential amplifier" *IEEE Journal of Solid State Circuits, VOL 44, NO. 5, May2009*

Appendices

APPENDIX

HSPICE – Analog simulation tool

HSPICE is SPICE based simulation tool which is popularly used in industry for performing numerical convergence, assists the latest device and offer measurements and optimization of circuits. The acronym SPICE depicts Simulation Program with Integrated Circuit Emphasis. When circuit to be simulated is formatted in a special syntax (HSPICE net list syntax) with defined supply sources, then numerical routine will do the analysis and represent numerical or graphical results desired by user. This simulation basically involves three steps:

- Generating netlist of the circuit
- Running Simulation
- Printing and analysing the simulation results

For generating netlist any text editor software with extension (i.e. filename. sp) can be used and is composed up of statements incorporating circuit components, interconnections, device models, input signals, voltage and current sources, type of analysis(i.e. DC, AC, Transient) and output data format. In general netlist file structure is as follows:

Title (mandatory)

Circuit description

Sub-circuit description (optional)

Device models

Analysis

Output Format

.end (mandatory)

HSPICE Input File

- Designing of netlist (containing circuit elements, supply and so on)
- Statement giving details of library file used (optional)
- Type of Analysis (optioinal)
- Desired output details (optional)

Summary:

- HSPICE has a upper limit on number of characters used in input statement or equation of 1024 per line.
- The statement can be continued to next line by including (+) sign as first character in next line
- GND, GROUND, GND! and node 0 address to global ground in HSPICE
- Comments can be included anywhere in the file and are represented by (*).

HSPICE Output File

Simulation results are saved which are desired in output listing file and if command OPTION POST is mentioned in data files which can be seen using waveform viewer such as Cosmoscope.All the file concerning with a single design rest in single directory and are called by concatenating design name with suffix.

Defining Parameters

Parameters can be defined with .PARAM statement. These parameters have some associated value. An undefined .PARAM statement is illegal.

The following types of value can be assigned to parameters:

- Real Number(constant)
- Algebraic expressions containing real values
- Functions which are predefined
- Function which are defined by users
- Circuit value
- Model v

VITA

The author, Preeti Joshi was born on 25 February 1992 at Hardwar (Uttrakhand). She passed her high school and Intermediate examination from D.A.V Centenary Public School, Hardwar (affiliated to C.B.SE. Board), during the year 2006 and 2008, respectively. She earned her B.Tech. degree in Electronics & Communication Engineering from Tula's Institute, Dehradun (affiliated to U.T.U) in 2012 in first division. She took admission in the college of Post Graduate Studies in G.B. Pant University of Agriculture and Technology, Pantnagar in July 2015, for Master's Degree in Electronics and Communication Engineering.

Permanent Address:

Preeti Joshi
C/O- Gokul Chandra Joshi
Gyanlok Colony
Kankhal
Hardwar
Uttrakhand, INDIA
Phone - +91 8449894156
Email: joshipreeti6@gmail.com

ABSTRACT

Name	:	Preeti Joshi	Id. No.	:	49400
Semester and Year of Admission	:	I^{st,} 2015-17	Degree	:	M.Tech.
Department	:	Electronics & Communication Engineering			
Major	:	Electronics and Communication Engineering			
Thesis title	:	Comprehensive Study of CNTFET based Positive Feedback Differential Amplifier			
Advisor	:	Dr. K. K. Sharma			

Regular Feature Size scaling down in today's CMOS technologies has led to the supply voltage reduction in order to cut short the level of consumed power while maintaining the device reliability that is by preventing gate oxide breakage. In highly scaled processes variations in device parameters increases, which makes CMOS poor performer.

The promising new transistor Carbon Nanotube avoids most of the limitations for MOSFET with its ballistic transport and ultra-long mean free path that make it suitable to work at sub-micron regime. These devices due to their small dimensions, shows large variations in their behaviour.

In this Study, various parameters differential amplifiers at 32nm are evaluated using CMOS and CNTFET technology and a comparison has been drawn between them for different circuits of differential amplifier and it has been found that CMOS Positive Feedback Differential amplifier gives highest gain and large Bandwidth which get further improved when CNTFET is used for CMOS thus improving the performance of the circuit.

(K.K. Sharma)
Advisor

(Preeti Joshi)
Author

सारांश

नम	: प्रीति जोशी	परिचयांक सं.	: 49400
षठ्मास एवं प्रवेश वर्ष	: प्रथम, 2015–16	उपाधि	: प्रौद्योगिकी में परास्नातक
प्रमुख विषय	:	विभाग	: इलैक्ट्रॉनिक्स एवं संचार अभियांत्रिकी
शोध शीर्षक	: काम्प्रीहेनसिव स्टडी ऑफ सी.एन.टी.एफ.ई.टी. बेस्ड पोसिटिव फीडबैक डिफ्रेनसियल एम्पलीफायर सी.एन.टी.एफ.ई.टी. आधारित सकारात्मक प्रतिक्रिया अंतर एम्पलीफायर के व्यापक अध्ययन		
सलाहकार	: डॉ0 के0के0शर्मा		

आज की सीमोस प्रौद्योगिकियों में स्केलिंग नियमित फीचर आकार ने आपूर्ति की वोल्टेज में कमी की वजह से डिवाइस की विश्वसनीयता को बनाए रखते हुए खपत बिजली का स्तर कम करने के लिए गेट ऑक्साइड टूटने को रोकने के लिए किया है। अत्यधिक स्केल किए गए प्रक्रियाओं में डिवाइस पैरामीटर में भिन्नता बढ़ जाती है जिससे सीमोस का प्रदर्शन खराब हो जाता है।

होनहार नए ट्रांजिस्टर कार्बन नैनोट्यूब मोसफेट के लिए अपनी बैलिस्टिक ट्रांसपोर्ट और अति लंबी औसत मार्ग है जो उप माइक्रोन शासन में काम करने के लिए उपयुक्त बनाता है। ये उपकरण को अपने छोटे आयामों के कारण, उनके व्यवहार में बड़े बदलाव दिखाते हैं। इस अध्ययन में 32 एन.एम. पर विभिन्न आयामों के विभेदक एम्पलीफायरों का मूल्यांकन सीमोस और सी.एन.टी.एफ.ई.टी. प्रौद्योगिकी के द्वारा किया गया है और अंतर एम्पलीफायर के विभिन्न सर्किट के लिए उन दोनों के बीच तुलना की गई है और यह पाया गया है कि सीमोस सकारात्मक प्रतिक्रिया विभेदक एम्पलीफायर उच्चतम लाभ और बड़ी बैडविड्थ देता है जो कि सी.एन.टी.एफ.ई.टी. का प्रयोग करने से और सुधर जाता है जिससे सर्किट के प्रदर्शन में सुधार होता है।

(के0के0शर्मा)
सलाहकार

(प्रीति जोशी)
लेखिका