Performance Evaluation of 22nm and 14nm TG-FinFET using Parametric Analysis

Thesis

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By

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I may lack at words when I sit and vent my gratitude but I find no other alternative to repay the debt of others who stood beside me throughout the completion journey of this work.

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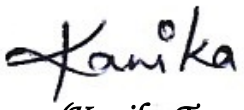

Pantnagar *(Kanika Tewari)*
November, 2020 *Authoress*

CERTIFICATE

This is to certify that the thesis entitled **"Performance evaluation of 22nm and 14nm TG-FinFET using parametric analysis"** submitted in partial fulfilment of the requirements for the degree of **Master of Technology** in **Electronics and Communication Engineering** of the College of Post Graduate Studies, G. B. Pant University of Agriculture and Technology, Pantnagar, is a record of *bona fide* research carried out by **Ms. Kanika Tewari,** Id. No. **54091** under my supervision and no part of the thesis has been submitted for any other degree or diploma.

The assistance and help received during the course of this investigation and source of literature have been duly acknowledged.

Pantnagar
November, 2020

(K. K. Sharma)
Chairman
Advisory Committee

CERTIFICATE

We, the undersigned, members of the Advisory Committee of **Ms. Kanika Tewari,** Id. No. **54091,** a candidate for the degree of **Master of Technology** in **Electronics and Communication Engineering**, agree that the thesis entitled **"Performance evaluation of 22nm and 14nm TG-FinFET using parametric analysis"** may be submitted in partial fulfilment of the requirements for the degree.

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Member

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Member

(Abhishek Yadav)
Member

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LIST OF ABBREVIATIONS

BJT	Bipolar Junction transistor
CMOS	Complementary Metal Oxide Semiconductor
DG-MOSFET	Double Gate Metal Oxide Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Type Metal Oxide Semiconductor
PMOS	P-Type Metal Oxide Semiconductor
SCE	Short Channel Effect
SOI	Silicon On Insulator
TG-FET	Triple Gate Field Effect Transistor
VLSI	Very Large Scale Integration

LIST OF SYMBOLS

nm	Nano Meter
μ	Mobility
C_{ox}	Oxide Capacitance
C_{si}	Silicon Capacitance
D	Drain
G	Gate
H_{fin}	Height Of Fin
L_g	Length Of Gate
N_a	Acceptor Charge Density
N_d	Donor Charge Density
S	Source
T_{ox}	Thickness Of Oxide Layer
V_g	Gate Voltage
V_t	Thermal Voltage
V_{th}	Threshold Voltage
W_{eff}	Effective Channel Width
W_{fin}	Width Of Fin
W_{foot}	Footprint Of The Substrate
ε_{ox}	Permittivity Of Gate Oxide

Introduction

The basic thing for the growth of Information technology is semiconductor electronics. Since the excessive demand of gadgets lead to a new revolution in VLSI technology. The application of VLSI technology is widely spread from a simple mobile to smart phones, Global positioning system (GPS), Defence and Military equipment, Satellites, Biomedical services and many other things which are not limited.

The journey of modern MOS (Metal Oxide Semiconductor) device was started in the year 1959 when Dawon Kahng and Martin M. John invented it in the Bell Labs. The Silicon MOSFET i.e. Metal Oxide Semiconductor Field Effect Transistor is the important semiconductor device in recent technology (**Figure 1.1 NMOS Device**) .The basic MOS is a 4 terminal device i.e. Gate (G), Drain (D), Source (S) and Body (B). It is used in monolithic Integrated circuits instead of Bipolar Junction Transistor (BJT) to perform the basic switching operations and amplification of electronic signals.

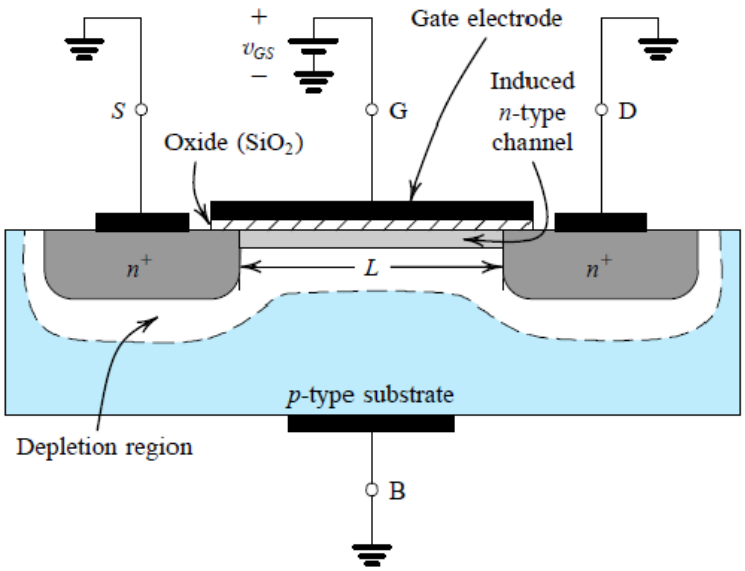


Fig.1.1: Schematic of N Type MOSFET [Ref. Sedra, A. S., *et al*, 1998]

Basically MOSFET is differentiated into two types (a) n channel MOSFET (b) p channel MOSFET where n channel MOSFET contains electrons in its channel whereas p channel MOSFET contains holes in its channel. Further, MOSFET can be operated in two modes (a) Enhancement mode (b) Depletion mode. Generally we use n

type enhancement mode MOSFET since NMOS is faster than PMOS due to mobility of charge carriers.

1.1 MOORE's Law

Gordon E. Moore in 1969 predicted that the number of transistors in chips doubles in every 18 months.

Limitation of Moore's Law

Gordon Moore on 13 April 2005 said that the law cannot be extended. He noticed that the transistors miniaturization limit reaches to the atomic levels. The basic barrier for this law is that the size of transistor is approaching to the size of atom.

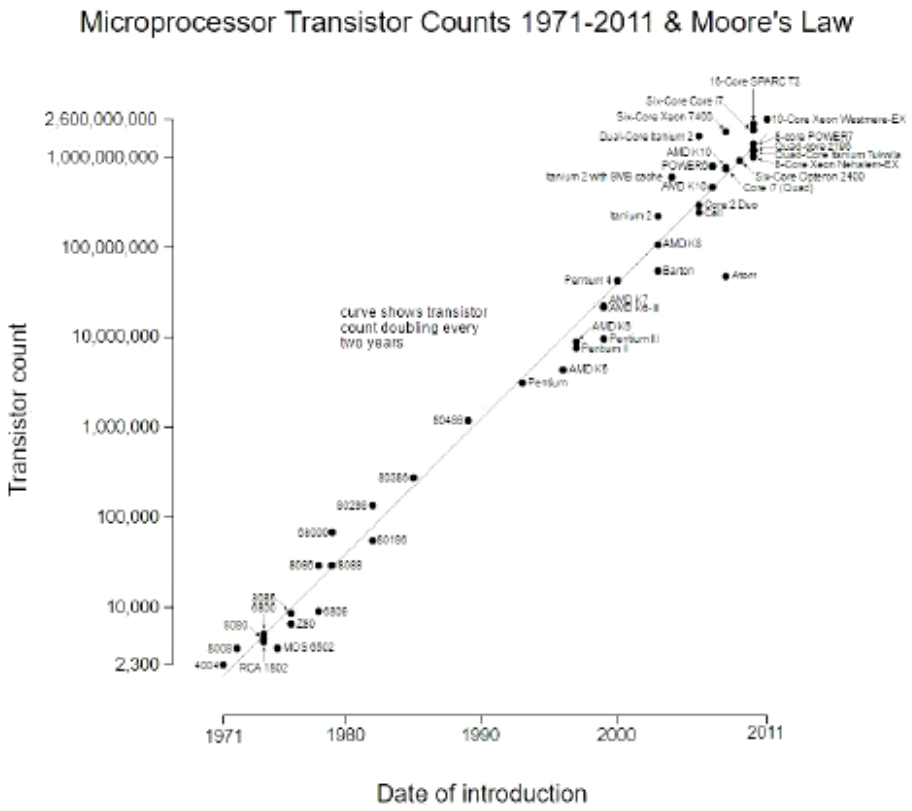


Fig1.2: Plot between transistor count and date of introduction of various IC's [Ref. Mittal, S., 2016]

1.2 Scaling of MOSFET

Scaling is a process of reducing the dimensions or the size of a MOSFET. The first comprehensive guidelines of scaling was "constant field scaling" theory that was given by **Dennard *et al.*** (**1974)** which states that, to boost the performance of a transistor, its dimensions and power supply should be reduced linearly whereas doping

concentration should go up in such a manner that the electric field remains at a constant value in the device. To satisfy Moore's law of doubling transistor in every 18 months the size of transistor also needs to decrease. Decreasing the size of all these parameters by a scaling factor S (S<1) will decrease the size of a MOSFET. As the dimension of a MOSFET is reduced, it is expected that the operational characteristics will also get changed and due to some limitations it confine the scaling of a transistor that we can achieve practically. The proportional scaling of devices will result in the reduction of total silicon area that is occupied by the circuit and thereby the functional density of chips gets increased.

It is desirable to scale the vertical as well as the lateral dimensions when decreasing the device size. The scaling affects both reliability and performance specifications of the process. Basically, there are 2 types of size reduction techniques

(a) Constant Field Scaling

- Vertical dimension decreases with the same lateral dimensions.
- To maintain fixed electric field, operating voltage decreases.

(b) Constant voltage Scaling

- Attractive due to electrical compatibility with existing circuit.
- Vertical dimensions decreases quadratically relative to the lateral dimensions.

1.3 Obstacles in Miniaturization of MOSFETs

To provide nanoelectronic devices with scaled MOSFETs, a few of the obstacles are as follows:

- Heat Dissipation: Due to the necessary limited thermodynamic efficiency, it limits the transistor density in circuit because overheating can cause malfunction.
- High Electric Field: Due to the applied bias voltage over very short distance, it can cause avalanche breakdown by knocking the large number of electrons out of the semiconductor at high energy, and hence causing current surges and damage to device.

- Vanishing Bulk Properties: On small scaled device, vanishing bulk properties and non-uniformity of doped semiconductor can be overcome either by a non-doping structure or by making the dopant atoms form a regular array.

1.4 Short Channel Effects

A MOSFET device is considered to be short when the length of channel is of same order of depletion layer width of drain (D) and source (S). As the length of channel becomes shorter, it enters into deep submicron region so various effects came into existences, which are known as short channel effects.

The short channel effects are attributed to 2 physical phenomenons (a) The limitation imposed on electron drift characteristics in the channel (b) The threshold voltage modification due to channel length shortening.

The different short channel effects are follows:

- Drain induced barrier lowering (DIBL)
- Punch through
- Subthreshold leakage
- Injection of hot carrier
- Velocity saturation
- Quantum effects

To overcome all the short channel effects several techniques have been introduced:

- Use of high-k dielectric material gate
- Silicon On Insulator (SOI) structure
- Strained Silicon Technique (S-Si) structure

1.4.1 High-k Dielectric Material gate

The parameter, dielectric constant defines the ability of a material to store charge. Consequently, it also defines the capacitance (C) comprising of a layer of dielectric sandwiched between two metal plates.

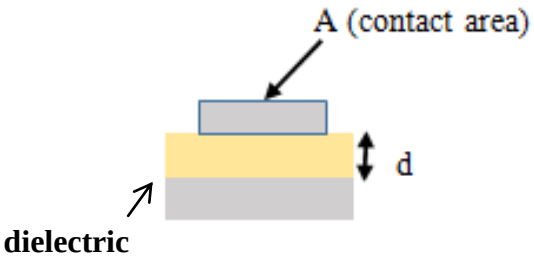


Fig.1.3: High-k dielectric gate

The capacitance can be found by using this equation:

$$C = \frac{\varepsilon_0 kA}{d}$$

The dielectric constant define the extent of capacitive coupling between two conducting plates with high-k dielectric material, such coupling would be strong and with low-k dielectric material being obviously weak. In Silicon technology, the reference value of dielectric constant (k) is taken as3.9 which refers to SiO2. Dielectrics having k>3.9 are referred as high-k dielectric materials that are needed in MOS gate stacks to maintain sufficiently high capacitance of the metal gate dielectric silicon structure.

1.4.2 Silicon on Insulator (SOI) MOSFET

Due to the scaling of dimensions and physical limitation of miniaturization, new devices came into existence. In SOI MOSFET a buried oxide is introduced, as shown in figure 1.4.

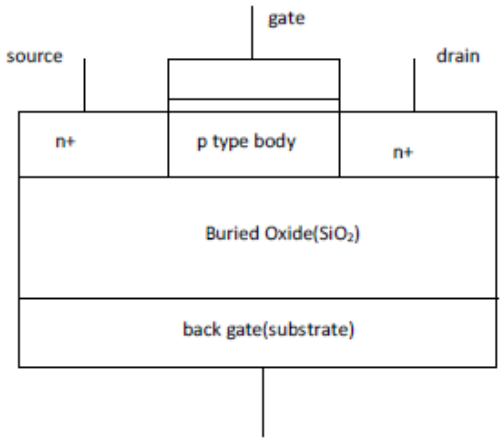


Fig.1.4: Schematic view of SOI MOSFET [Ref. Park, J.T. *et al*, 2002]

SOI MOSFET is of 2 types:

(a) Partially Depleted SOI

(b) Fully Depleted SOI

- **Partially depleted SOI (PD-SOI):** In this type of MOSFET, the thickness of silicon film is larger than the sum of width of depletion region from the back to the front end. Hence there is no interaction takes place between drain/source and the buried oxide, as a result of this a neutral piece remains beneath the depletion region. If that piece is connected to body or ground than it will work as Bulk MOSFET, but if that piece is not connected to any of the contact, than it gives rise to kink effect and degrade the device characteristics.

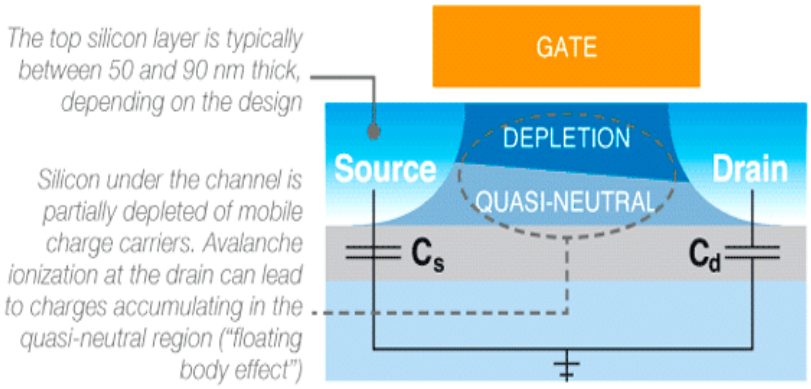


Fig.1.5: Cross-section of Partially depleted SOI-MOSFET [Ref. Park, J.T. *et al*, 2002]

- **Fully Depleted SOI (FD-SOI):** In this type of SOI MOSFET the interaction between drain/source and buried oxide takes place and hence no neutral piece exists there, as a result of this kink effect is eliminated. This technology is suitable for the nodes 22nm and beyond for high performance microprocessor and low power electronics.

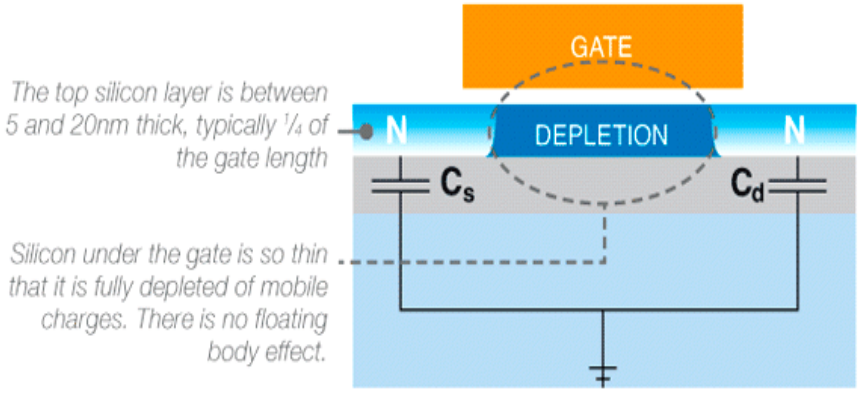


Fig.1.6: Cross-section of Fully depleted SOI-MOSFET [Ref. Park, J.T. *et al*, 2002]

1.4.3 Strained Semiconductor Films

The strain in crystalline solid is due to the relative displacement of atoms in the lattice. The strain creates proportional distortion of key material properties of semiconductor including the band gap and the effective mass of an electron in the strained region is reduced hence the mobility gets increased. Consequently, creation of strain in the transistor region where electron mobility has an effect in determining the performance will result in faster switching transistor.

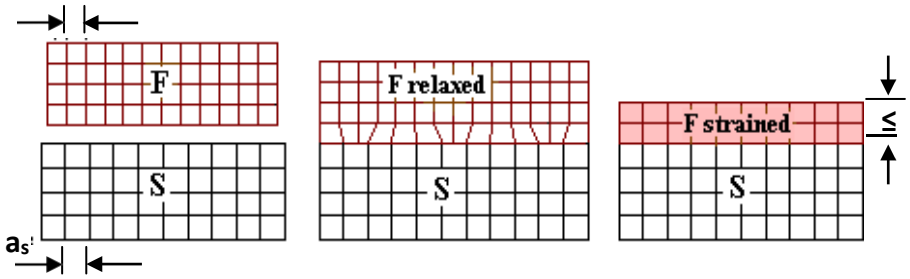


Fig.1.7: Formation of Strain on Silicon Wafer [Ref. Veshala, M. *et al*, 2013]

Due to the performance improving properties, the lattice mismatched semiconductor hetero-structures contains strained films that rare rapidly growing in semiconductor device technology.

1.5 Advanced Nano-Scaled Devices

Due to the scaling of dimensions and physical limitation of miniaturization, new devices came into existence.

1.5.1 Double Gate MOSFET

The concept of Double Gate MOSFET (DG-MOSFET) came into existence by the concept of back biasing in bulk MOSFET as the threshold voltage is controlled by the back gate biasing. It has 2 gates (a) front gate (b) back gate, as shown in figure 1.8. Both gates simultaneously control the charge at silicon and oxide interface.

The advantage of Double gate MOSFET is less short channel effects. There are 2 types of Double gate MOSFET:

a) Symmetry Type: In this type both gates having same work function, so that at the same gate voltage both surface channels turned ON.

b) Asymmetry Type: In this type both gates having different work functions also, at the threshold voltage only one channel will turn ON.

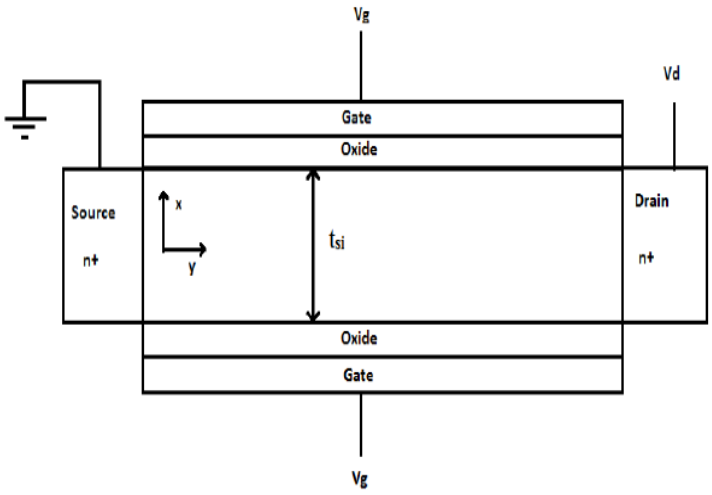
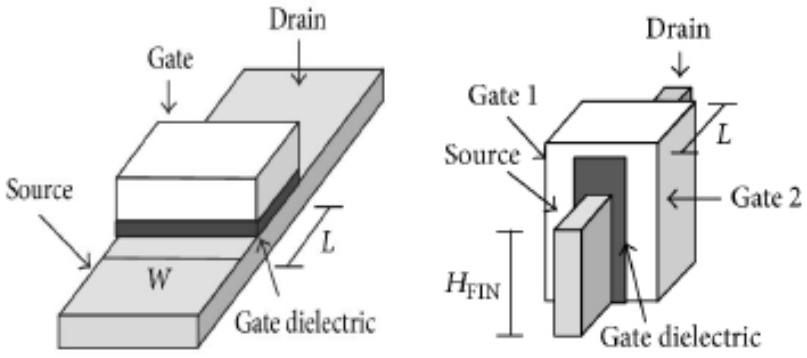


Fig.1.8: Schematic view of DG-MOSFET [Ref. Singh, D. *et al*, 2015]

1.5.2 FinFET

As the technology is scaled down, the device characteristics of MOSFET gets degraded, so to replace the conventional CMOS transistor in different electronic circuits a new device FinFET was used. To explain the non-planar double gate electronics structure, to overcome the physical scaling limitations in nanometer regime the term FinFET was introduced by **Hisamoto *et al*. (2000).** In a FinFET the channel is raised up into a 'fin' with the gate wrapped around it. The comparison between the Planar MOSFET and FinFET is shown in figure 1.9



(a) Planar MOSFET **(b) FinFET**

Fig.1.9: Comparison between Planar MOSFET and FinFET [Ref. Bhattacharya, D. *et al*, 2014]

FinFETs can also be differentiated as SOI FinFET and Bulk FinFET. In SOI FinFET the fin is built over the oxide and hence completely isolated from the substrate whereas in bulk FinFET the fin is connected to the substrate through the oxide layer. The schematic view of FinFET is shown in figure 1.10.

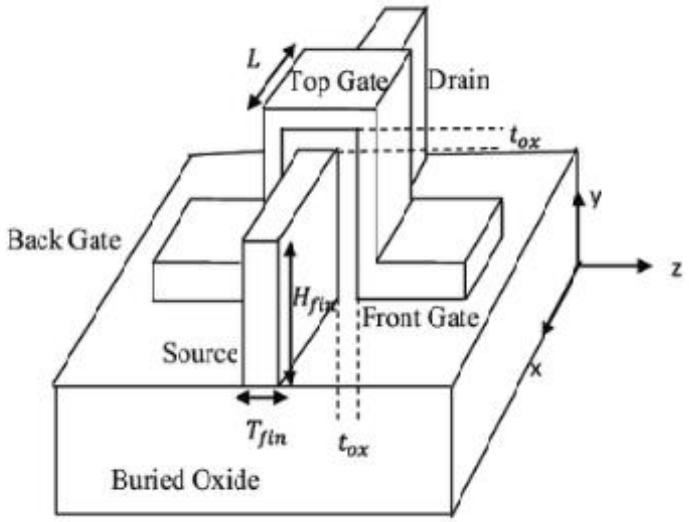


Fig. 1.10: Schematic view of FinFET [Ref. Yang, W. *et al*, 2007]

Advantages of FinFET over CMOS

- Superior gate control of the channel even at the low voltage.
- Highly reduced Short Channel Effects.
- Better performance for a given power budget.
- Highly integration density due to 3D structure.
- FinFETs have lower DIBL, hence it reduce subthreshold leakage.
- Works at low operating voltage.
- High operating speed.

Disadvantages of FinFET over CMOS

- FinFETs are complex device to model.
- Accurate FinFET parasitic extraction is more complicated.
- The body biasing technique that is commonly used in planar MOSFET is less effective in FinFET.

1.5.3 Multigate FinFET

In a fully depleted mode, the Multigate FinFET actively permits to control the short channel effects rather than the other. This happens because of the close coupling of capacitors of the multiple gates of FinFET to the channel area from the different directions. As the number of gates increases, the control of gate becomes stronger. In DG FinFET the thickness of gate oxide at top portion of fin is large, hence only two gates remain to be in effect for channel control, while in TG FinFET the channel is formed at both top surface and side wall surfaces, due to this the drive current increases. So, as compared to DG FinFET, TG FinFET is better implemented and also has high on current (drive current). Since the fabrication of TG FinFET is easy as compared to DG FinFET hence they are emerging as the dominant structure device for future technologies. The three dimensional structure and the cross sectional view of tri-gate FinFET (TG-FinFET) is shown in the figure 1.11.

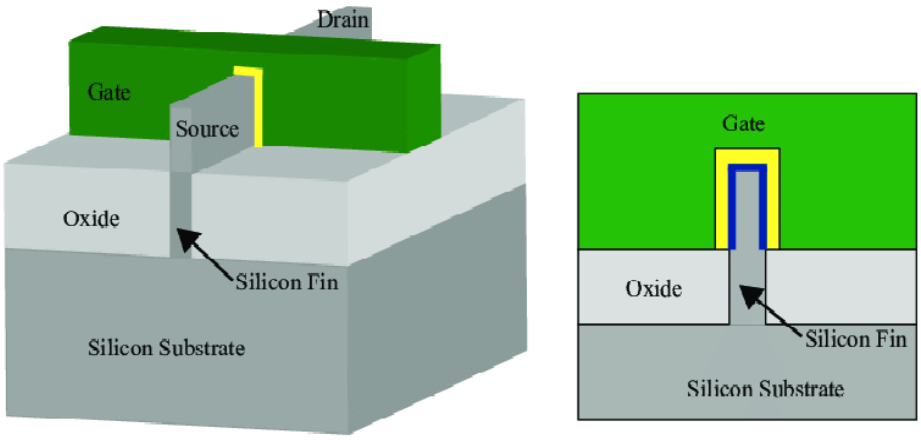


Fig. 1.11: Tri-gate FinFET Structure (3D structure & cross sectional view), [Ref. Revathy, G. *et al*, 2014]

1.6 Motivation

For the several years, scaling of technology has given us improved circuit performance and reduced cost per function but the industry faces many challenges as CMOS scales down to 45nm technology node and beyond, such as, gate oxide tunnelling, increased leakage current and short channel effects (SCEs). In order to reduce the off state leakage current, the depletion width of channel must be reduced which results in high doping that also reduces the mobility of charge carrier. To enhance the performance and maintain the threshold voltage of device, the thickness of

gate oxide must be scaled along with the channel length. Hence to overcome the shortcomings of MOSFET a new device structure FinFET was introduced. In FinFET, a thin Si fin is wrapped around the conducting channel that forms the body of the device. Among the different structures of FinFET i.e. DG-FinFET and TG-FinFET, TG-FinFET offers high drive current, low leakage current, less power dissipation and better immunity to SCEs. So, TG-FinFET device for lower technology node has emerged as the dominant structure.

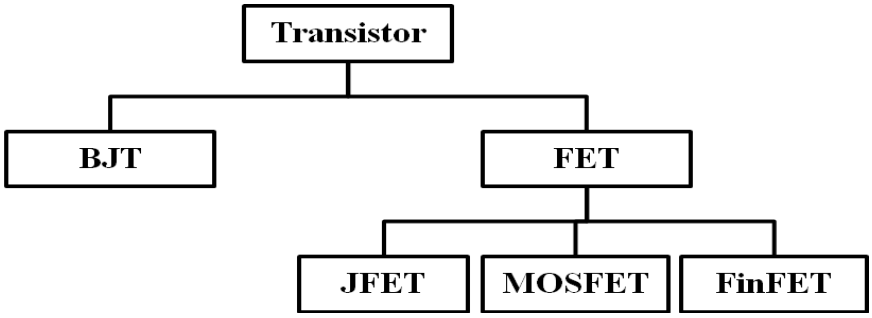


Fig. 1.12: Classification of Transistor

1.7 Problem Statement

In this work the main aim is to implement the device structure at technology node 22nm and 14nm for different dielectric material and analyse its performance based on the drive current capability, leakage current, power dissipation and short channel effects for different parameters. The problem of present work has been stated as **"Performance evaluation of 22nm and 14nm TG-FinFET using parametric analysis"**.

1.8 Research Objective

The objective of this research work proposed is:

1. To design and simulate 22nm FinFET for low k-dielectric material.
2. To design and simulate 22nm FinFET for high k-dielectric material.
3. To design and simulate 14nm FinFET for low k-dielectric material.
4. To design and simulate 14nm FinFET for high k-dielectric material.
5. To compare the performance of device based on different variable parameters such as doping concentration, oxide thickness, fin height, fin width and length of underlap.

1.9 Outline of Thesis

To have the better understanding of the topic and to obtain the purpose of the work a brief review of literature has been given in the next chapter (Chapter 2). After the literature review, the basic concepts related to FinFET and its different structures were discussed under a separate chapter materials and methods (Chapter 3). Then the TCAD simulation results and analysis have been reported for different technology node in the chapter (Chapter 4). Then at last the summary and conclusion has been drawn from the presented work (Chapter 5).

Review of Literature

Chapter 2 REVIEW OF LITERATURE

As discussed in the first chapter, the problem of research has been taken from the CMOS and FinFET technology. A literature review regarding the CMOS and FinFET for different scaled technology node has been again taken into consideration. The problem due to the downscaling of technology node in MOSFET devices causes the emergence of new device structure that can overcome its shortcomings, are also reviewed and separately explained here.

Researchers have found that FinFETs are the new device structure in this emerging technological era that can overcome the shortcomings of planar devices. The main focus of this research work is on different scaled technology nodes of FinFET device. A review of FinFET device has also been discussed in order to cater the need of material and method used by the prominent researchers.

Hence, the chapter "Review of Literature" is categorized as follows:

I. CMOS device Scaling and issues

II. New emerging device "FinFET"

2.1 CMOS device Scaling and issues

Chan *et al.* (1987) have investigated that, the main cause of downscaling of CMOS technology is due the effect of Gate induced drain leakage (GIDL), in which the drain leakage current is detected at the drain voltage that is much lower than the breakdown voltage. The flow of current is due to the gate induced electric field in the gate to drain overlap region and dominating drain leakage current as gate voltage is zero in the thin oxide MOSFET. Hence, in the sub-micron region, the Gate induced drain leakage current is an important problem where the thickness of gate oxide is less. Also, the voltage required to cause band to band tunneling process caused by the high electric field in the gate oxide region, hence for the present and future device designs, an exact oxide thickness and doping profile should be preferred for the drain/gate overlap region.

Wann *et al.* (1996) have elaborated that, as the technology advances to high scalability, the MOSFET device structures continuously give good performance and

less cost to the integrated semiconductor chips. The motivation behind the scaling of device not only includes the good performance but also less consumption of power for the system on chip. This discussion includes the analytical models that are used for the optimization of MOS devices and also to compare other device structures under the same constraints. MOSFET device includes Delta doped MOSFET, Uniformly doped substrate, Partially depleted SOI MOSFET, Fully depleted SOI MOSFET, Double gate MOSFET. All these devices are compared on the basis of some parameters that are Threshold voltage control, subthreshold swing (SS), Saturation current, Capacitance and SCEs.

Gonzalez *et al.* (1997) have investigated how the effect of reducing supply voltage and threshold voltage is beneficial by using a delay and energy model of first order CMOS circuit. The effect is shown to be advantageous when the used transistors are velocity saturated and also the nodes have high activity factor. Scaling of supply voltage can lead to poor performance. Whereas, the scaling of threshold voltage can confined the performance loss but accelerate the static power dissipation. Operation in the subthreshold region is favourable if one parameter is optimized for the minimum energy. For the measure of circuit efficiency the energy delay product (EDP) is used. For low power operation, the low operating voltage seems to be very appealing but it is very sensitive to manufacture and operating point variations. Hence, the supply voltage and threshold voltage is scaled to the extent so that it assert constant electric field within the device.

Gordon E. Moore (1998) concentrated on the scaling of the device. The statement provided under this is "With the falling of unit cost, the number of components per circuit increases". The economics of 1975 dictates the squeezing of as many as 65,000 components on a single Si chip. By the Integrated electronics it is suggested that all the technologies that are referred to as microelectronics as well as any additional ones that results in electronics function supplied to the user as irreducible units. Finally, the proposed Moore's law states that "The number of transistors in a dense integrated chip gets doubles in approximately every two years".

Hisamoto *et al.* (2000) have proposed a new Double gate self-aligned MOSFET structure which is based on the Delta structure. For the ultra-thin body device, the desired threshold voltage was achieved by using the gate material which is

boron doped. In this structure the channel was formed on the surface (vertical side) of Silicon fin and the current starts to flow parallel to the wafer surface. This gate channel gate stacked structure is realized by the quasiplanar technology. Since the gate is self-aligned to Source/Drain, due to which the parasitic resistance got raised.

Godoy *et al.* (2001) have presented a new method to find the subthreshold swing (SS) of short channel SOI and bulk MOSFET. For the submicron ranging dimensions, this methodology utilizes the channel potential expression. As the device gets scaled down the short channel effects (SCEs) are considered progressively important because of the lateral field penetration in channel region, due to which the threshold voltage gets degraded and the subthreshold swing gets increased. The subthreshold swing model for short channel devices is derived for three structures i.e. bulk MOSFET, thin film fully depleted MOSFET and double gate SOI MOSFET. With this model, the increase in accelerated subthreshold swing (SS) is observed for the scaled devices.

Frank *et al.* (2001) have presented the factors that limit the continuous downscaling of Si CMOS technology and provided the analysis in which application related consideration enter under these limitations. The origin of these limitations are basically in the tunnelling currents that starts leaking through different MOSFET barriers, as the technology gets downscaled. Also, these leakage currents depend upon the geometry of MOSFET along with the designing criteria that are required for minimizing the short channel effects. Leakage currents that came into effect from the applications that are related to power consumption and functionality of circuit, limits the scaling of device. Finally, how the constraints work out for applications like DRAM, SRAM, low power portable device and high performance CMOS logic were discussed.

Park *et al.* (2002) have proposed an easily manufacturable tri gate device (Π-gate fully depleted SOI MOSFET) whose side walls are extended into the buried oxide. In buried oxide, the extended side walls of the gate material produces a pseudo gate or field induced back gate that efficiently enhances the drive current and protect the back of channel from electric field lines that comes from drain. The simulation was performed by taking four different device parameters that are channel width, silicon film thickness, gate length and doping concentration. The proposed tri gate device offers some short channel properties which are very near to a GAA MOSFET. In

comparison to the DG devices, subthreshold swing and optimum design space of the Π-gate device were also examined. The result shows that in tri gate device, as the device width is increased, the efficiency of lateral gates decreases and the when the thickness of silicon film is increased, the gate control of DG devices decreases.

Roy *et al.* (2003) have explained the reason of intrinsic large leakage phenomenon in the scaled down MOS transistor, that has become the main cause of power consumption of the device. As the technology gets scaled down, different short channel effects arises due to which the leakage current increases hence the leakage power in the device gets increased. This paper analyses the different device leakage process that comprise Drain induced barrier lowering (DIBL), Gate induced drain leakage (GIDL), weak inversion and gate oxide tunnelling effect. Channel engineering method comprise retrograde well and halo doping is examined to reduce the short channel effects for constant scaling of MOS transistor.

Wu *et al.* (2007) have examined the progression on partially depleted SOI (PDSOI) modelling that utilizes the surface potential base method. The newly designed model is known as "PSP Model" that is constructed within the present current standard of conventional MOS device PSP Model. Also, besides this physics based approach and scalability inheritance from PSP, PSP SOI apprehend SOI precise effects using the inclusion of floating body simulation capacity, parasitic bipolar model and self-heating. The PSP SOI model is verified over various PDSOI technologies.

2.2 New Emerging device "FinFET"

Woo *et al.* (2002) have investigated the outgrowth of non-uniform source/drain doping profile on FinFET device characteristics by using 3D device simulation. When the doping profile for source/drain is fixed, then because of the coexistence of large channel region the high silicon on insulator thickness suppresses the short channel effects (SCEs). Due to these reduced short channel effects some design margins in the channel can be considered. To find out the suitable thickness of silicon on insulator its AC characteristics are also investigated. With silicon on insulator thickness, device capacitance also increases but in gate delay case, as the drive current also gets increase and recompense the increase of capacitance. Finally, it is observed that the device having large drain current or high silicon on insulator thickness are more advantageous for the fixed source/drain doping profile condition.

Kedzierski *et al.* (2003) have fabricated double gate (DG) FinFET device architecture of high performance whose gate length is as small as 30nm. In the fabrication process the main focus was on the reduction of parasitic series resistance. The methods to minimize the parasitic series resistance were angled extension implants and selective silicon epitaxy raised source/drain, by which the high performance of device can be obtained. The extension resistance was observed to be a function of fin thickness (T_{Fin}). For fin thickness less than 25nm (T_{Fin}<25nm) the extension resistance increases rapidly. The FinFET device optimization was done not only for the short channel effects (SCEs) reduction by reducing the fin thickness but also consider the reduction in I_{on}/I_{off} due to the high parasitic resistance. FinFETs that have fins in <100> directions have higher NMOS transconductance and go towards having high silicon epitaxy growth rate. Whereas, FinFETs that have fins in <110> directions have higher PMOS transconductance. Also, the issues like fin epitaxy, spacer formation, fin orientation were discussed.

Havaldar *et al.* (2006) have studied the variation of threshold voltage and subthreshold slope along with the device geometry and also the doping concentration in the channel. The potential variation is obtained by the use of 3D Poisson's equation to calculate the threshold voltage and subthreshold current in FinFET device for both doped and undoped channels. For the same device geometry, the undoped channel gives high carrier mobility and the channel doping allow better control over the threshold voltage (V_{th}) and the short channel effects (SCEs) get reduced. Also, the model for threshold voltage of mesa-isolated small geometry FD-SOI MOSFETs is reported, that is based on the solution of three dimensional Poisson's equation. This model can be used for the FinFET design and for the circuit simulation purpose.

Yang *et al.* (2007) have presented a scaling theory of FinFET that has been set up by three dimensional analytical solutions and also the numerical simulation of Poisson's equation in the channel region. The analytical solution of three dimensional Poisson's equation in the doped channel is obtained by the use of superposition method in channel and source/drain respectively. On the basis of this analysis the expression for minimum channel potential is derived from the evanescent mode which is a simple and useful subthreshold swing (SS) model. With the given geometrical values a demonstrable expression is given to forecast the values of subthreshold swing. Also, for optimization the ratio of channel length to the scaling length should be greater than three is required.

Sachid *et al.* (2008) have presented a phenomenon named as Gate fringe induced barrier lowering (GFIBL) in FinFET devices having the undoped underlap regions, since it is difficult to fabricate and precisely control the defined doping profiles in Source/Drain underlap regions. As the technology gets scaled down, that FinFET device having gate overlap shows high off current (I_{Off}) that needs to be optimized very carefully. Hence, the use of underlap with optimized doping profile came into existence. Also, the usage of underlap that is undoped with source/drain junctions find appealing for future technology nodes. To enhance the GFIBL effect, the use of high k spacers in such devices is also proposed that helps in achieving better device and circuit performance. Use of high k spacers improves the drive current (I_{on}) of the device by approximately 80% and for the fan-out of four the inverter delay gets decreased by 15%.

Saini *et al.* (2010) have analysed the effect of high k-dielectric in FinFET devices. By the use of high k-dielectric, the leakage current of device is improved and also the performance gets increased. The simulation results show that while doing the adjustment of threshold voltage, work function plays a vital role in it.

Kloes *et al.* (2010) have proposed a coherent current equation for lightly doped devices for both below and above the threshold operation. In the operation of below threshold the mobile charge is directly framed from the 3D model. Whereas, in the above threshold operation the inversion charge is calculated from the standard MOS equation, that uses a 3D model to determine the electrical parameters such as DIBL, threshold voltage and subthreshold slope. To define a single current equation both operations can be combined for multigate field effect transistor. This approach is found to be reasonable till the time the effects of quasi ballistic transport and quantum confinement are neglected. Also, this model correctly forecast the influence of the channel geometry on device current and transconductance. Due to its simplicity it can be applied for a numerical efficient implementation in circuit simulators and also by the use of 3D analytical model its physical insight is maintained for the electrostatic potential that define electric parameters of the device.

Saini *et al.* (2011) have analysed the scaling limits of FinFET device for Double Gate underlap and Triple Gate overlap structure. The simulation of different structures was performed using fin height, fin thickness and gate length as variables using 2D and 3D computer simulation. For 2D simulation of double gate FinFET, gate length (L) and fin thickness (T_{Fin}) are responsible for the device performance. As (L/T_{Fin}) ratio goes below 1.5, DIBL and SS abruptly got increase. Whereas, For 3D

simulation of triple gate FinFET, Fin height (H_{Fin}) and Fin thickness (T_{Fin}) are responsible. Here, the (L_{eff}/T_{Fin}) ratio can go below 1.5 for the same short channel effects unlike the double gate FinFET. The obtained simulation results show that the tri-gate FinFET is more scalable than the double gate FinFET. For the analysis of good performance of the device structure H_{Fin} and T_{Fin} needs to be carefully optimized as increasing the H_{Fin} value degrade the fin stability which further increases the difficulty in patterning of gate and also degrades the short channel effects.

Hossain *et al.* (2011) have discussed that scaling the size of MOSFET has great influence on its electrostatic characteristics. The electrostatic characteristics include such as current, voltage and effective mobility variation with effective electric field. The distinguished characteristics of FinFET device is due to the conducting channel that is wrapped up by a thin Si film known as "fin" hence forming the gate of the device. The variations of these characteristics lead to the divergence effect that is essential for the designing and manufacturing point of view. With thin Si film, at high electric field mobility degradation has been observed, which can further leads to Volume inversion.

Bukkawar *et al.* (2012) have presented a Source and drain over insulator (SDOI) FinFET device structure, where the source/drain regions are insulated from the body. The insulation is done by the buried oxide with an undoped, underlap and dielectric, which is taken as Si_3N_4. The result of presented structure shows that the SDOI FinFET device with underlap and Si_3N_4 as dielectric has lower leakage current than the SDOI FinFET device with underlap and SiO_2 as dielectric. Also, the DIBL of SDOI FinFET device with Si_3N_4 as dielectric gets reduced and the ratio of drive current to leakage current gets increased, as compared to SiO_2 as dielectric.

Saremi *et al.* (2012) have proposed a FinFET device structure to reduce the DIBL effect that invokes two ground planes under the source and drain. Also, how the coupling of electric field between source and drain is reduced by the ground plane (GP), to decrease the Drain induced barrier lowering (DIBL) was discussed. In the SC SOI device ground plane method is one of the methods that are used to decrease the DIBL. If the distance between ground plane and drain is negligible in comparison to the channel length, than ground plane (GP) method is suitable. The performance between GP-FinFET to Bulk FinFET and SOI FinFET were compared, which showed that in the proposed structure, DIBL and leakage current gets reduced, the ratio of the saturation current to leakage current gets increased, and the subthreshold-swing gets improved.

Fasarakis *et al.* (2012) have presented a compact drain current model for lightly doped or un-doped short channel tri-gate FinFET, considering the quantum mechanical effects (QMEs) and short channel effects (SCEs) i.e. DIBL, Threshold voltage shifting and degradation of subthreshold slope. For tri-gate FinFET different analytical approaches have been developed to calculate the electrostatic potential within the channel, based on this model the threshold voltage, scaled short channel characteristics of subthreshold slope and DIBL were obtained. Also, the proposed Π-shaped FinFET is limited to linear region and channel length less than 40nm, but the model symmetry and good accuracy makes it suitable for circuit simulation.

Tripathi *et al.* (2012) have proposed the Pie-gate bulk FinFET device that is suitable for the logic applications for the requirement of SOC. The impact of gate at bottom to depth of junction, misalignment was investigated for deeper and shallower junctions. In this proposed pie-gate structure the deeper gate electrode has more control over the bottom of the fin and also due to its electrostatic control the subthreshold performance of the device gets enhanced. This explained bulk pie-gate FinFET device with source/drain to body junction narrow than the gate at bottom has equal or better threshold performance than SOI FinFET.

Soman *et al.* (2013) have proposed a drain-extended triple gate FinFET, that contains better hot carrier reliability, which results in increase in drive current and decrease in the leakage current and hence the ratio of drive current to leakage current gets increased. The drain region of tri-gate FinFET structure is extended by the addition of a drift region between the drain and the channel of the device. In this extended drain drift region the majority of electric field gets trapped instead of trapping at the channel region and causing hot carrier effect in the extended region. Therefore, it provides better hot carrier reliability and reduced leakage current.

Veshala *et al.* (2013) have analysed how the short channel effects can be reduced by using FinFET device. The scaling of bulk devices requires such methods that avoid the constraints of conventional MOSFET device. The short channel effects are limited by the physical structure and the off state leakage is controlled by using ultra-thin Si film in FinFET. For reduction of leakage current, the thickness of Si film should be less than one-fourth of the length of channel. Also, the threshold voltage can be changed by changing the gate work function using the mid gap material.

Revathy. G *et al.* (2014) have illustrated that how the gate covered the channel from all the three sides and how the source and drain embossed on the substrate. This multi gate FinFET overcomes the limitation of CMOS transistor technology such as leakage current and short channel effects. FinFET has proved to be more efficient than the CMOS in terms of performance but still the parasitic capacitance of the CMOS is better than that of FinFET. Due to this, the switching speed of the device gets reduced. The operating modes of FinFET decide upon how many gates can control the channel. In Independent gate mode, the two gates separately control the channel, whereas in Shorted gate mode just as CMOS both gates have their own parasitic capacitance, due to the overlap of gate-drain and gate-source. Then, even a FINFET has its parasitic capacitance more than that of CMOS as the gate is covered all 3 sides.

Singh *et al.* (2015) have compared the simulated results for both DG-MOSFET and FinFET as the underlap length is varied. Presently the integrated device manufacturer (IDM), electronic design automation (EDA) companies and foundries grant more emphasis on multi gate technology. So, sensitivity of underlap length on AC and DC parameters like subthreshold swing, drain current, delay, transition frequency and electronic device automation is studied for both the devices. FinFET device demonstrates better result than the DG-MOSFET device in case of immunity to leakage current and hence intrinsic delay, intrinsic source delay inductance and power dissipation also get improved. It is because the FinFET design has a better control on the channel that shows better immunization capability towards the short channel effects.

Mishra *et al.* (2015) have construed the 22nm FinFET device performance for different gate material under different oxides at 0.5V of supply voltage. The drain current with different work function and different gate material has been observed. The high k dielectric material (HfO2) is used to reduce the short channel effects, and high k dielectric along with metal gate is used to get high device performance.

Chauhan *et al.* (2015) have described the modelling result of p-type Ge-FinFET by using the BSIM-CMG model technology. For the fabrication of FinFET devices, Ge can be used for performance enhancement of P-type FinFET since the mobility of holes in Ge is higher, in the similar manner Si or III-V material group is

used in N-type FinFET as the mobility of electrons is higher. With the updated industrial standard compact model the Si N-FinFET and Ge P-FinFET can be modelled so accurately. Here, the scalability of BSIM-CMG model is proposed where, the global parameter extraction is done for different gate length.

Hajare *et al.* (2015) have discussed the performance analysis of FinFET based digital circuits at 22nm and 14nm technology node. As the technology gets scaled down the performance of MOSFET is also get reduced hence the limitation of MOSFET is overcome by the use of FinFET device. The result obtained for the digital application at 22nm and 14 nm show system trade off. Also, as the technology gets scaled from 22nm to 14nm the device cover less area and the power dissipation is reduced. Hence the FinFET devices possess better performance than the MOSFET device.

Kaur *et al.* (2016) have investigated the impact of various process parameters such as thickness of gate oxide, ratio of H_{fin} to W_{fin} on the performance of tapered FinFET of gate length 20nm. The Density gradient quantum correction model is used to include quantum mechanical effects that become significant at gate length of 20nm. The Performance has been measured in terms of subthreshold swing (SS), drive current (I_{on}), leakage current (I_{off}), and drain induced barrier lowering (DIBL). For different combinations of input process parameters, these output parameters are compared. Tapered FinFET shows performance advantage for narrow fins but not for much taller fins. For low power applications this tapered Triple Gate FinFET can provide optimized performance.

Abraham *et al.* (2017) have examined the 22nm multigate bulk FinFET structure with two different dielectric materials, since at this technology node the conventional MOSFET has reached its limitation of having high leakage current and also the poor performance. In the presented FinFET structure, due to the reduction of gate dielectric material it has reached to the limit of large increase of gate leakage current which is caused due to the tunnelling effect. When low k dielectric material (SiO_2) is used, due to further scaling, leakage current will increase resulting in the increment of power consumption. In order to overcome the limitations of low k dielectric material (SiO_2) the high k dielectric material (HfO_2) is used which results in

reduction of leakage current, better stability, less power consumption and the ratio of drive current to leakage current gets increased, which is required for the low power operation. Also, the capacitance extraction has been done to analyse the performance of these two dielectric materials.

Shukla *et al.* (2017) have analysed that in deep submicron technology the scaling of technology is performed by scaling the gate length and oxide thickness and this can be achieved by changing the MOSFET structure to FinFET structure. In FinFET the better electrical control is provided by the wrap around gate structure, which makes it a multigate device and hence the leakage current and short channel effects gets reduced. For the industrial purpose the top fin width is reduced which results in better gate control over the channel and improvement in the device performance. Also, in deep submicron technology, the quantum effects become significant. Hence, in design simulation the density gradient model is used which incorporates the considerable quantum effects.

Verma *et al.* (2019) have compared the performance of 20nm FinFET device at different dielectric materials. As compare to low k-dielectric material, the high k-dielectric material shows 1.41% improvement in potential voltage at low gate voltage, whereas in case of high gate voltage 0.98% of improvement has been obtained. Also, when gate voltage is low, 15% improvement in the energy conduction band and when gate voltage is high, 14% improvement has been observed. By the use of high k-dielectric material, leakage current is reduced, better potential distribution is observed and also the short channel effects get reduced.

Verma *et al.* (2020) have presented a 14nm FinFET model. Further the device performance has been observed considering different parameters such as temperature variation, variation of oxide thickness and different dielectric materials. The result shows that as compare to k-dielectric, the high current ratio is observed as high k-dielectric, hence the switching speed of device gets enhanced, also the power dissipation get improved upto 38% than in low k-dielectric material.

After the brief literature survey the summary of various technology nodes are given in the tabular form. The performance of the device is analysed at supply voltage depending upon the technology node.

Table 2.1: Different technological nodes given by different researchers

Reference	Technology node	Supply voltage
Woo *et al.* (2002)	30nm	1V
Kedzierski *et al.* (2003)	30nm	1.5V
Sachid *et al.* (2008)	20nm	1V
Kloes *et al.* (2010)	30nm	1V
Saini *et al.* (2011)	47nm	1V
Bukkawar *et al.* (2012)	30nm	1V
Saremi *et al.* (2012)	50nm	1V
Tripathi *et al.* (2012)	32nm	1V
Soman *et al.* (2013)	22nm	1V
Singh *et al.* (2015)	22nm	0.7V
Mishra *et al.* (2015)	22nm	0.5V
Hajare *et al.* (2015)	22nm	0.9V
	14nm	0.8V
Kaur *et al.* (2016)	20nm	1V
Abraham *et al.* (2017)	22nm	0.8V
Shukla *et al.* (2017)	20nm	1V
Verma *et al.* (2019)	20nm	1V
Verma *et al.* (2020)	14nm	0.8V

In this research work the device is designed at 22nm and 14nm technological node at a supply of 1.2V for different dielectric material. The simulation results were obtained using the Cogenda Visual TCAD tool. In the next chapter the device material and working methodology has been explained.

Materials and Methods

As discussed in the second chapter, the main emphasis of researchers was on the scaling of device with increment in the number of transistors per chip area. But with the downscaling of technology the performance of conventional MOSFET degrades as the leakage current of device increases also various short channel effects come under consideration. Hence, to reduce the effect of short channel effects in bulk MOSFET and SOI MOSFETs, Double gate MOSFET (DG-MOSFET) has been introduced. Though DG-MOSFET suppresses many of these effects but the difficulty in fabrication has been encountered due to the misalignment of top gate and back gate. Hence to overcome these difficulties i.e. misalignment of gates, FinFET architecture has been introduced for future generation transistor technologies.

3.1 FinFET

The term FinFET was introduced by Hisamoto *et al.,* U C Berkley researchers in 2000. The main distinguishing characteristics of the FinFET is that the conducting channel is wrapped by a thin silicon i.e. fin, which forms the body of the device. The effective channel length of the device is determined by the thickness of the fin i.e. from source to drain. The working of the FinFET is similar to conventional MOSFET. In a FinFET the channel is raised up into a 'fin' with the gate wrapped around it in a 3D structure as shown in figure 3.1.

Where,

H_{Fin}: Height of fin

W_{Fin}: Width of fin

L_g: Length of gate

There are 2 types of FinFET (a) DG FinFET (b) TG FinFET

In DG FinFET, only two gates control the channel whereas, in TG FinFET the channel is formed at top surface and also at both side walls hence the areal density of on state current gets increased that result in the performance enhancement of the device. Therefore, with the ease of fabrication and high performance of TG FinFET, they are emerging as the dominant device structures for future technology.

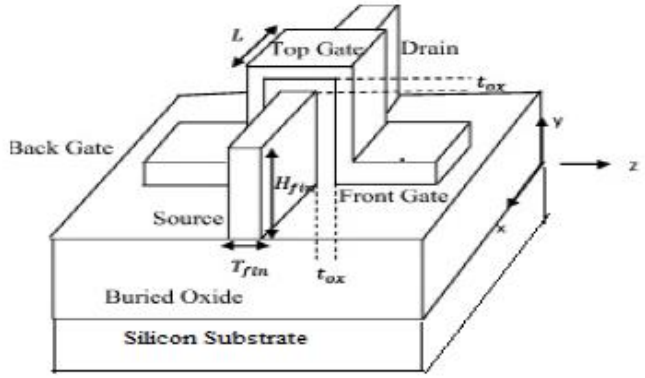


Fig. 3.1: Schematic of FinFET [Ref. Yang, W. *et al*, 2007]

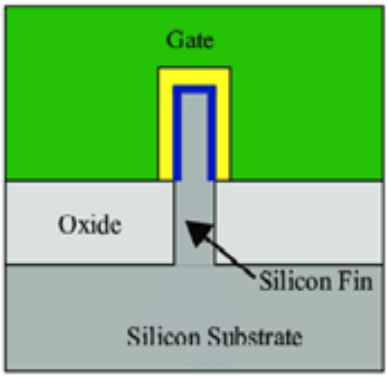
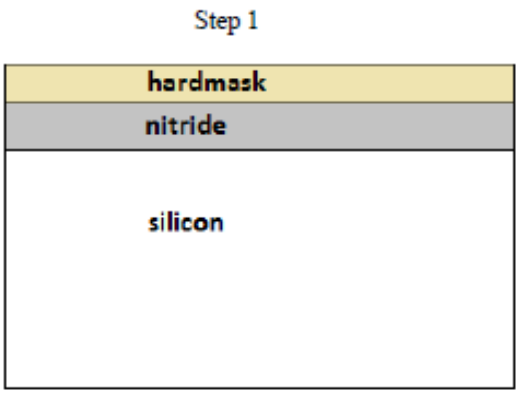


Fig. 3.2: Cross section along the Fin [Ref. Revathy, G. *et al*, 2014]

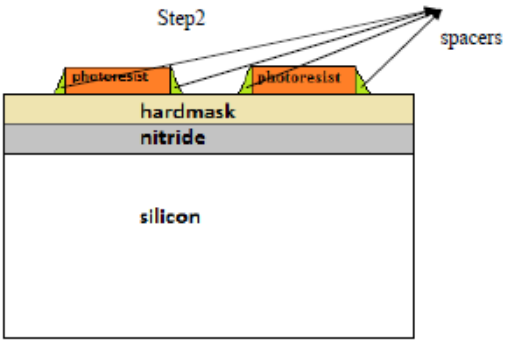
3.1.1 Fabrication of FinFET

One of the methods of fabrication of FinFET is Subtractive method. The steps of fabrication of FinFET are follows:

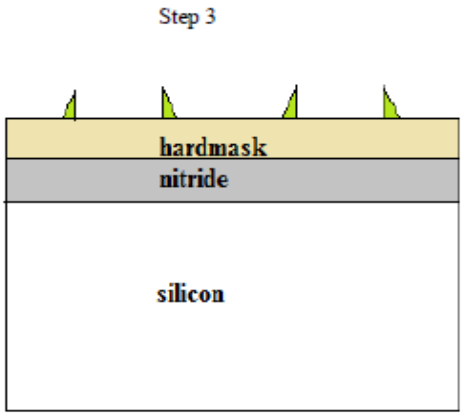
1. Grow the silicon nitride as capping of silicon layer and then hardmask it.



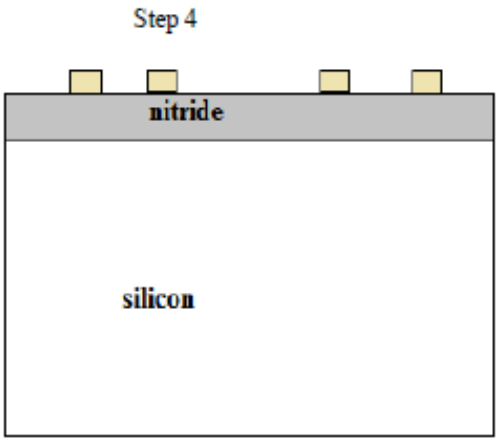
2. Now add photoresist material and then spacers are grown.



3. The photoresist material is removed and the device remains with nitride as spacer.

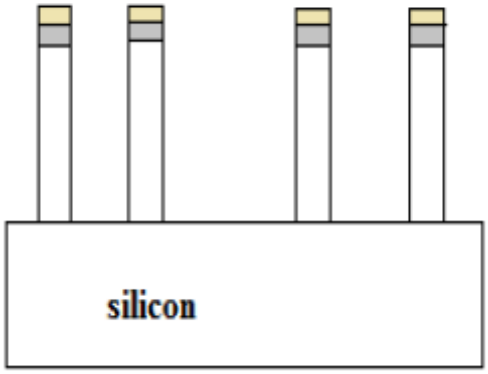


4. The nitride is itched so that the hardmask remains which protects the silicon below it.



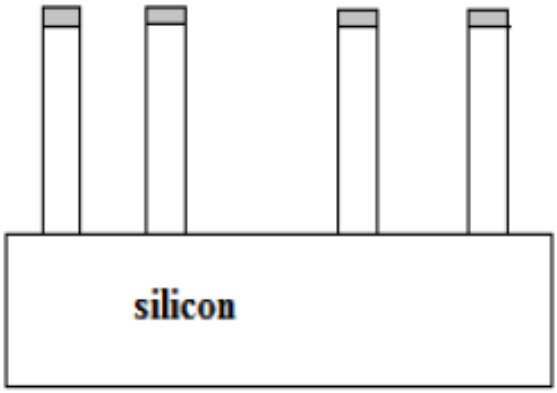
5. After etching, the area below hardmask remains unetched forming fin.

Step 5



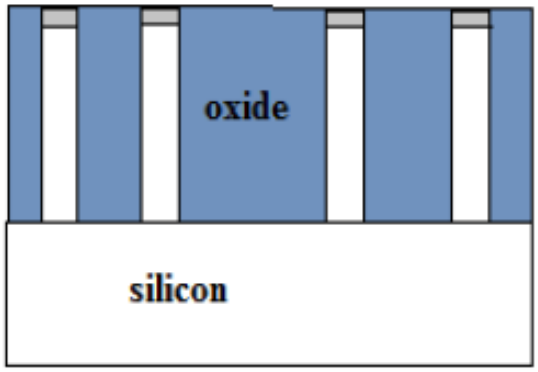
6. The Remaining hardmask is then etched.

Step 6

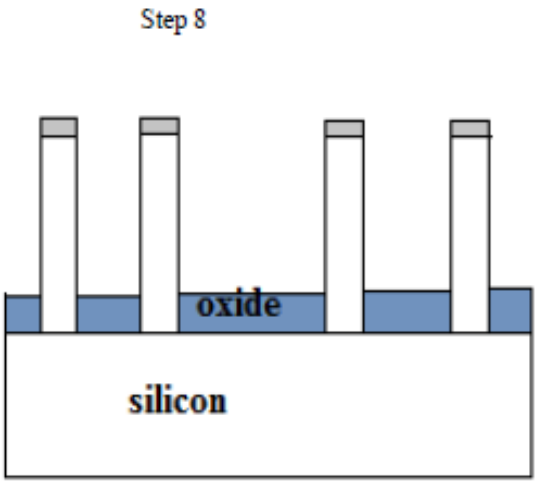


7. The gaps between fins have been filled with oxide and then the top portion is planarized.

Step 7



8. Then oxide is etched according to the height of fin.



3.1.2 Different structures of FinFET

On the basis of wrapping of gate electrode around the channel region, the different structures of FinFET are following

(a) SOI FinFET: In this type, the hard mask is a thick dielectric that prevents the formation of an inversion channel at the top of silicon fin. Gate control is exerted on the channel from lateral sides of the device.

(b) SOI Tri-gate MOSFET: In this type, the gate control is exerted on the channel from three sides (top, left side, right side).

(c) SOI Π-gate MOSFET: The gate control is imposed over the tri-gate MOSFET, because the electric field from the lateral sides of the gate exerts some control on the bottom side of the channel.

(d) SOI Ω-gate MOSFET: The gate control of the bottom of the channel region is better than in the SOI Π-gate MOSFET. The name Ω-gate and Π-gate tells about the shape of the gates.

(e) SOI gate all-around MOSFET: The gate control is exerted on the channel from four sides of the device.

(f) Bulk tri-gate MOSFET: In this type, the buried oxide is underneath the device, also the gate control is exerted on the channel from three sides.

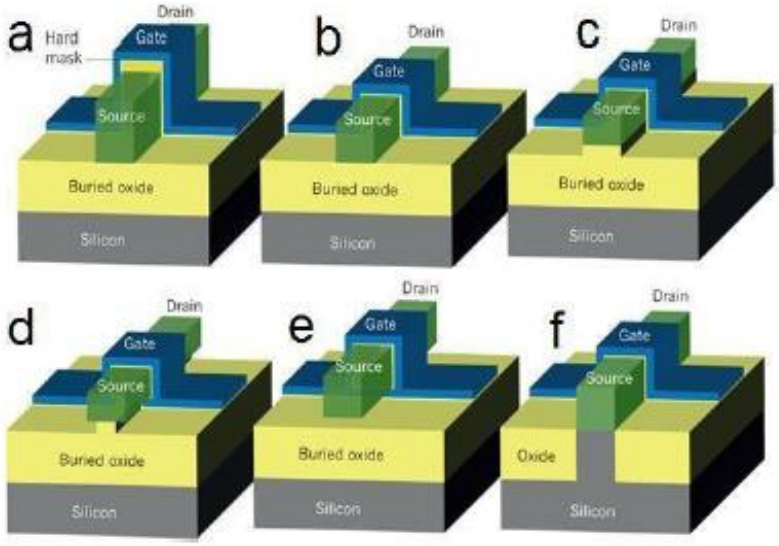


Fig.3.3: Different structures of FinFET [Ref. Sonone, S. *et al*, 2017]

3.1.3 Active area of FinFET: Fins

I. Fin Width (W_{Fin}): As the gate length is shrinking continuously, the drain starts to compete with the gate electrode to control the channel potential. Due to the scaling of device many short channel effects came into effect, which are 1. A Threshold voltage roll off 2. Higher subthreshold leakage 3. Punch Through between drain and source when $V_{DS}= V_{DD}$. The method of controlling short channel effects is to use two or more gate electrodes and a thin fully depleted semiconductor body. This is done to amplify the potential curvature in the source and drain direction, by making a large electric field gradient in the direction which is vertical to the gate. The key parameter is the thickness of fully depleted thin semiconductor body and this thickness is called Fin Width.

There are other methods that reduce short channel effects but then we have to deal with the detrimental side effects of those methods. Such methods include

1. Gate oxide thickness reduction: This leads to higher gate to channel capacitance.
2. Higher channel doping: Due to this, the charge sharing in channel between the gate and drain reduces and causes large potential barrier between source and drain. It also reduces the carrier mobility and increases the Gate induced drain leakage (GIDL).

II. **Fin Height (H_{Fin}) and Fin Pitch (P_{Fin}):** In case of a Double-gate FinFET, the channels are on the sidewall of the fins. Hence the effective channel width is:

$$W_{eff} = 2n*H_{Fin}$$

Where,

n= number of fins

The fin pitch is defined as the spacing between the fins plus the fin width. It is limited by the lithography pattern capability. At one P_{Fin}, exactly one fin can be placed.

Therefore the effective channel width per pitch is: $2*H_{Fin}$.

The comparison between planar MOSFET and FinFET is shown in fig. 3.4

For the planar MOSFET, the effective channel width W_{eff} is:

$W_{eff} = W_{foot}$, where W_{foot} is the footprint of the substrate

For the FinFET, the effective channel width is $W_{eff\ is}$:

$$W_{eff} = 2 * H_{Fin} * \left(\frac{W_{foot}}{P_{Fin}}\right)$$

If FinFET layout is desired to be Competitive,

$W_{eff} \geq W_{foot}$ Or $2*H_{Fin} \geq P_{Fin}$

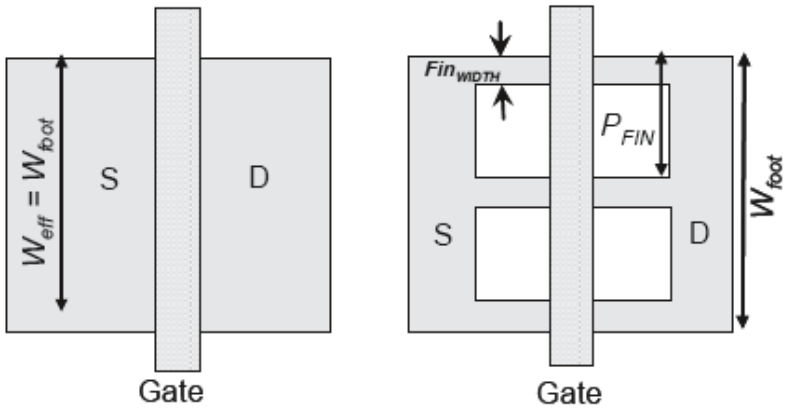


Fig.3.4: Layout comparison between a planar MOSFET and FinFET [Ref. Sonone, S. *et al*, 2017]

3.1.4 Analysis of current flow and current model for tri-gate FinFET

As the channel length gets shorter, the potential barrier across the cross-section of channel gets increased because in long channel devices, the potential is mainly

controlled by the gate surrounding the channel from all three sides, whereas in the short channel devices the potentials of drain/source influence the barrier height.

In tri-gate FinFET, during the weak inversion most leaky path exists in the bottom center of the channel because for low gate voltage, the effect of gate decreases as one goes away from the gate. The gate covers channel through three sides (top, left and right), thus the leakiest path exists at bottom center, which is far from all three gates and the effect of drain potential is higher at the point shown in fig., due to which firstly, the channel forms at the bottom center. Fig.3.5 shows that along the width of fin, the potential increases and at the bottom, it attains maximum value. Fig. 3.6 shows that along the height of fin, the potential increases and at the bottom, it attains maximum value and from both the graphs it is clear that the leakiest path exist at the bottom center of the fin. As we increase the gate voltage, the channel starts moving from bottom center to oxide interface. In tri-gate FinFET, as the height of fin becomes greater than width of fin, each half of the top gate width along with the side gates, contribute for channel formation.

Hence the effective width: $W_{eff} = H_{Fin} + W_{Fin}/2$

The overall current of Tri-gate FinFET with channel length modulation (CLM) is represented as:

$$I_d = \mu_0 \frac{2W_{eff}}{L} \frac{\varepsilon_{ox}}{t_{ox}} (2V_t)^2 \left[(q_{is} - q_{id}) + \frac{1}{2}(q_{is}^2 - q_{id}^2) \right]$$

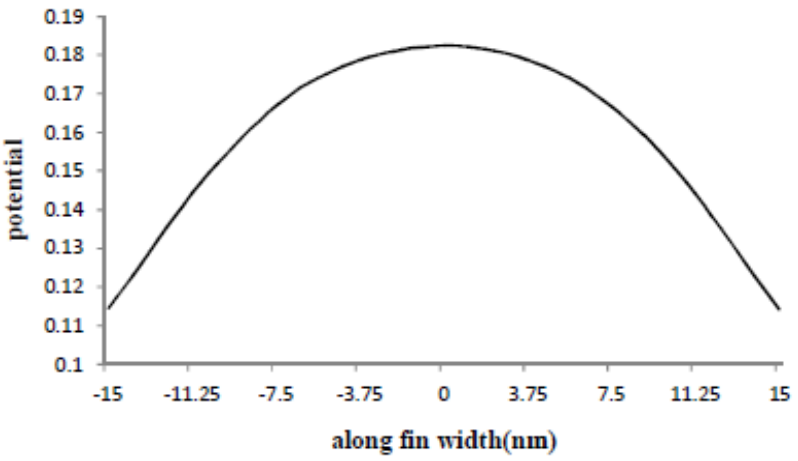


Fig.3.5: Potential graph at weak inversion along the fin width

Where,

μ_0 : Low field electron mobility

ε_{ox} : Permittivity of gate oxide

V_t : Thermal voltage

q_{is} : Sheet charge density calculated at source side

q_{id} : Sheet charge density calculated at drain side

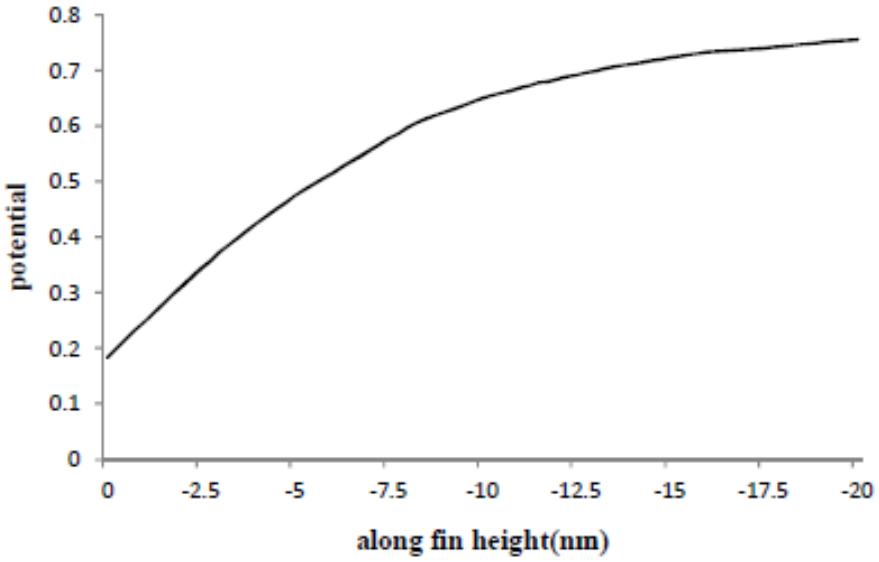


Fig.3.6: Potential graph at weak inversion along the fin height

The sheet charge density can be find as:

$$q_{ix} = Lambert\, W_{eff}\left(e^{\frac{(V_g - V_{th} - V_x)}{2V_t}} \frac{e^{\frac{(V_g - V_{th} - V_x)}{2\eta_{TG}' V_t}}}{A + e^{\frac{(V_g - V_{th} - V_x)}{2\eta_{TG}' V_t}}} \right)$$

Where,

$A = 4e^{\frac{V_t + V_{fb}}{V_0}}$

V_x : channel voltage at source 0

V_{th} : Threshold voltage

V_t : Thermal voltage

The Threshold voltage is given as:

$$V_{th} = V_{fb} - \frac{A_{1,TG}(V_{bi} + V_d) + A_{2,TG}V_{bi}}{1 - (A_{1,TG} - A_{2,TG})} + \frac{V_{th}}{1 - (A_{1,TG} - A_{2,TG})} \ln\left(\frac{Q_{th}N_a}{n_i^2 W_{fin}}\right)$$

Where,

$V_{fb} = \Phi_{ms} - V_{th}\ln(N_a/n_i)$, is flat band voltage

Φ_{ms} : Work function difference between silicon and metal

V_{bi} : $V_{th}\ln(N_a/n_i)$, is Built in potential

When the substrate is highly doped, than the effect of depletion charges came into effect, which affects the built in potential as well as threshold voltage. Thus the modified V_{th} and V_{bi} are :

$$V_{th} = V_{fb} - \frac{A_{1,TG}(V_{bi} + V_d) + A_{2,TG}V_{bi}}{1 - (A_{1,TG} - A_{2,TG})} + \frac{V_{th}}{1 - (A_{1,TG} - A_{2,TG})} + Q_d$$

Where,

Q_d =0.5*q*$N_{a*}W_{Fin}$

and

V_{bi}: $V_{th}\ln(N_a N_d/n_i^2)$, here N_a=Acceptor charge density and N_d=Donor charge density

$A_{1,TG}$ and $A_{2,TG}$ are the parameters, that are functions of natural length and channel length, also for short channel devices these parameters have some finite values whereas for long channel device these values are 0.

Q_{th} is the minimum sheet charge density, that is required to achieve turn ON of strong inversion and it is given as:

$$Q_{th} = \frac{2V_{th}}{q} * \frac{C_{ox}^2}{C_{si}}$$

Where,

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, oxide capacitance

$C_{si} = \frac{\varepsilon_{si}}{W_{Fin}}$, silicon capacitance

For single fin FinFET, the graph between gate voltage and drain current is shown in fig.3.7

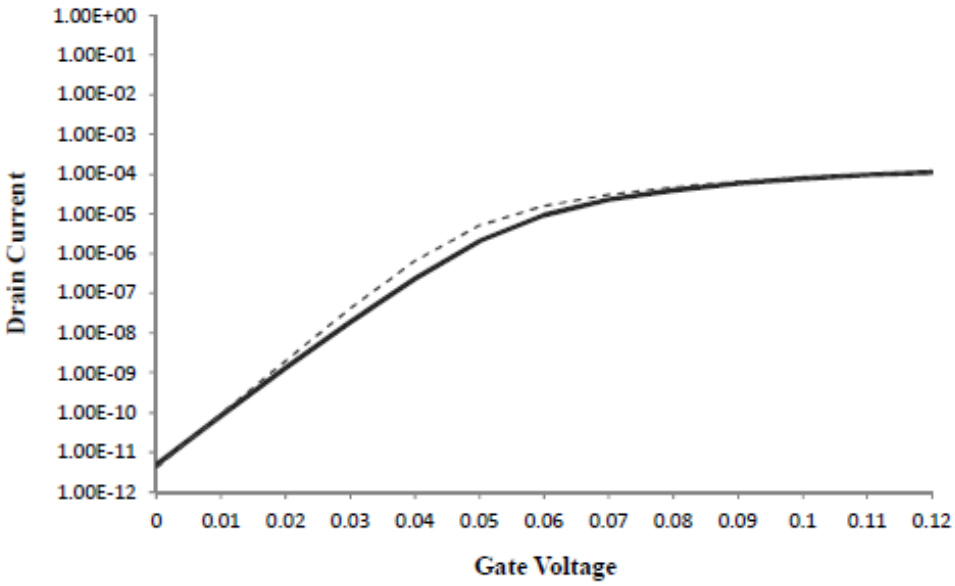


Fig.3.7: Drain current versus gate voltage at V_d=0.8 and t_{ox}=1.2nm

Where,

Dashed line represents the simulation result and solid line represents the model result.

3.1.5 Gate oxide material

It is a dielectric layer that separates the gate terminal of device to the conducting channel that connects the source and drain terminal when transistor is turned ON. The earliest gate dielectric used in a field effect transistor was SiO_2. SiO_2 is the key reason of using Si in microelectronics because of its excellent insulator properties. SiO2 has the key advantage that it can be made from silicon by thermal oxidation, whereas every other semiconductor has a poor native oxide. SiO2 is amorphous and has very few electronic defects and it forms an excellent interface with Si. It can be etched and patterned to a nanometer scale. The problem of using SiO_2 arises when thin oxide thickness is required. Since the gate oxide leakage is increasing with decrease in SiO2 thickness and SiO2 is running out of atoms for further scaling that increases leakage current which in turn increases the power consumption. Hence the use of high-k dielectric material arises. The new dielectric materials should have the following characteristics:

1. It must have high enough k that will be used for reasonable number of years of scaling.
2. It must form a good electrical interface with Silicon.

3. It must be kinetically stable with silicon channel.
4. The dielectric must be in direct contact with silicon channel so it must be thermodynamically stable with it.

The gate dielectric is subject to many constraints such as high capacitance to increase the transconductance and high thickness to avoid the dielectric breakdown. The thickness and Capacitance constraints are almost directly opposed to each other. High-k dielectric materials exhibit excellent characteristics like high permittivity, high barrier height, compatibility with different gate materials, and reduction in leakage current and better stability over silicon material. These properties make high-k materials suitable candidates to replace SiO2. Replacing SiO2 with a dielectric material having high dielectric constant will definitely improve the oxide capacitance. As a result leakage current will be reduced; this will give a better stability and low power consumption. So high k materials for gate oxide, increases the on-off current ratio of the device which is very essential for low power operation. Hafnium oxide (HfO_2) has been considered as an alternative to Silicon dioxide (SiO_2) since it provides the required capacitance at reduced device size because of its high dielectric constant i.e. k=25.

3.2 Proposed FinFET device

The basic structure of 3D FinFET device is similar to as shown in fig. 3.1 where the gate length is 22nm and 14nm. The parameters that can affect the performance of device are Fin height (H_{fin}), Fin width (W_{fin}), Gate length (L_g) and Gate oxide thickness (tox).

3.2.1 Structure design of 22nm device

Table 3.1: Device Parameters used for simulation of 22nm FinFET

Parameter	Value
Channel length	22nm
Oxide thickness	1.2nm-1.6nm
Fin Height	10nm-20nm
Fin Width	5nm-15nm
Source/Drain Doping	1e20 cm^{-3}
Channel doping	1e15 cm^{-3}-1e19 cm^{-3}

Table 3.2: Device Parameters used for simulation of 14nm FinFET

Parameter	Value
Channel length	14nm
Oxide thickness	0.8nm-1.2nm
Fin Height	10nm-20nm
Fin Width	5nm-15nm
Source/Drain Doping	1e20 cm^{-3}
Channel doping	1e15 cm^{-3}-1e19 cm^{-3}

3.3 Methodology

The FinFET structure having different gate length 22nm and 14 nm was simulated using 3D simulator Cogenda Visual TCAD. Analysis of the structure has been done based on the parameters listed in Table 3.1 and 3.2. The structure is generated by writing the process code in TCAD. After writing the code, structure was simulated using different dielectric materials (SiO_2 and HfO_2).

3.3.1 Variation of parameters in FinFET Performance

1. Effect of doping concentration: FinFET's drain leakage current or off-current (Ioff) is the current when no gate voltage is applied. Drive current or on-current (Ion) is the current when gate voltage is maximum. The On-Off current ratio (Ion/Ioff) represents the power consumption of the device. As the doping concentration is increases, the On current decreases linearly and Off current decreases exponentially this leads to sharp increase in On-Off current ratio. Also, the DIBL and Subthreshold swing decreases with increase in doping concentration.

2. Effect of Fin height and Fin width: As the height and width of fin increases, both the drive current and leakage current increases. The On-current increases because of the increased channel inversion area and the Off-current increases because of the decrease in gate supremacy of the channel and this leads to the reduction of On-Off current ratio. Also, with the increase in height and width of fin the DIBL and subthreshold swing increases.

3. Effect of Underlap length: As the length of underlap increases, both the drive and leakage current decreases and hence the On-Off current ratio increases. Gate capacitance decreases due to underlapping but the resistance between Source and Drain increases and hence the performance of device may get enhanced.

4. Effect of dielectric material: With the use of high k-dielectric material the fringing field increases and it causes the barrier lowering in underlap regions that allows more carriers from source region to enter into the channel region which results in higher On-current of the device that leads to the improvement in device performance. Also as we move from low k-dielectric to high k-dielectric the value of DIBL and Subthreshold swing decreases.

3.3.2 Cogenda Visual TCAD Tool

Visual TCAD is the latest graphical user interface for the Genius device simulator that is designed to suit novice TCAD users and students, and focuses on ease of use. Using TCAD has never been as easy, no more command line or coding is required. Beginners will be able to get started within just a few minutes. On the other hand, it doesn't sacrifice the power of Genius. All the physical models and options are accessible with Visual TCAD.

Visual TCAD combines with the Genius Device Simulator to create a next-generation TCAD solution. Genius is a parallel 2D/3D TCAD device simulator, featuring a wide range of advanced physical models and simulation capabilities. Incorporating the latest parallel computation technology, the Genius Device Simulator is able to handle large problems with 200,000 or more mesh nodes and is capable of speeding up simulation times by a factor of 10 or more.

Results and Discussion

Chapter 4 RESULTS AND DISCUSSION

Simulations have been performed to find the effect of fin height, fin width, underlap length and different dielectric materials on the leakage current and device drive current using Cogenda Visual TCAD software over 3D FinFET as described and proposed in chapter Material and Methods. The data used for simulation were given in table 3.1 and 3.2.

As reported in literature review the doping concentration was found variations ranging from 1e15 to 1e19 out of which 5 variations has been selected for the study. Similarly based on the literature for oxide thickness variation we have considered 3 values in the range, 3 variations for height of fin, 3 variations for width of fin and 2 variations in underlap length in the range which have already been mentioned in the chapter 3 under table 3.1 & 3.2. Among all different gate oxide dielectric materials that are Silicon dioxide (SiO_2, k=3.9), Silicon oxynitride (SiON, k=7.9), Aluminium oxide (Al_2O_3, k=9), Yttrium oxide (Y_2O_3=15), Hafnium oxide (HfO_2, k=25) as studied in literature, we have selected SiO_2 for low-k dielectric material and HfO_2 for high-k dielectric material. The simulated results are shown into two broad categories:

1. Study of Id-Vgs characteristics
2. Study of variation of various process parameters

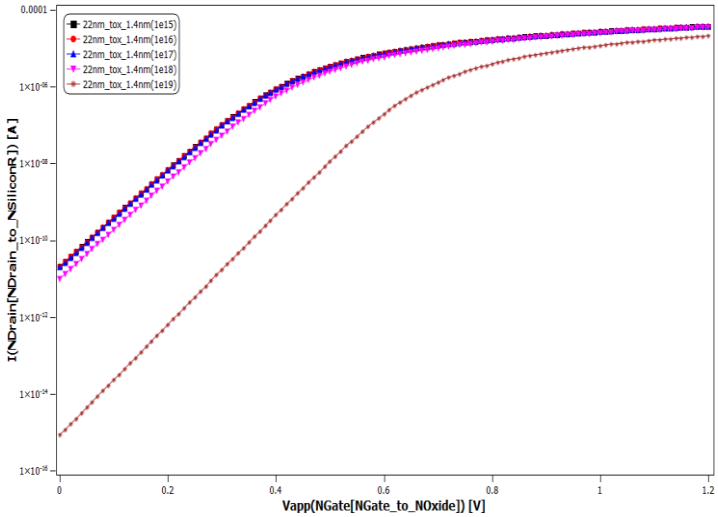
4.1 Study of Id-Vgs Characteristics

The drain current versus gate voltage curve shows drive current and leakage current of any device when plotted in logarithmic scale. When no gate voltage is applied the measured drain current is leakage current and when high voltage is applied the measured drain current is known as Drive current. The following graphs show the relation between drain current and gate voltage when doping concentration and oxide thickness has been varied.

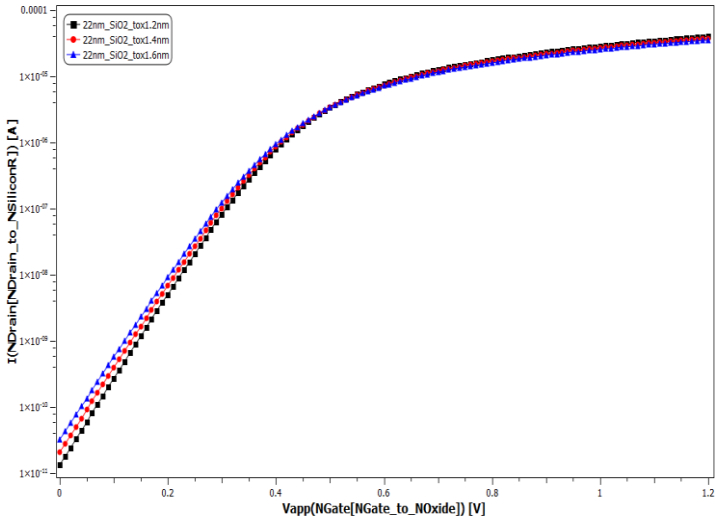
4.1.1 Id-Vgs characteristics for 22nm device using low k- dielectric

With 22nm low-k dielectric material, doping concentration and oxide thickness was varied. The result show that in case of high doping concentration i.e. 1e19 the leakage current (approx 8.378e-16) is much reduced than that in low doping concentration i.e. 1e15 (approx 2.072e-11) as depicted in figure 4.1(a). Also, figure

4.1(b) illustrates the variation of oxide thickness in which low leakage current is obtained at the lower oxide thickness i.e. 1.2nm than that in 1.6nm.



(a)



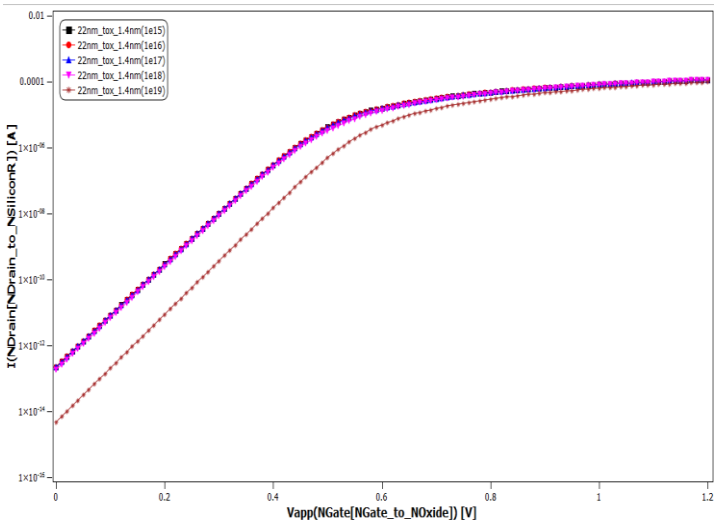
(b)

Fig. 4.1: Id-Vgs characteristics for low-k dielectric at 22nm for (a) different doping (b) different oxide thickness

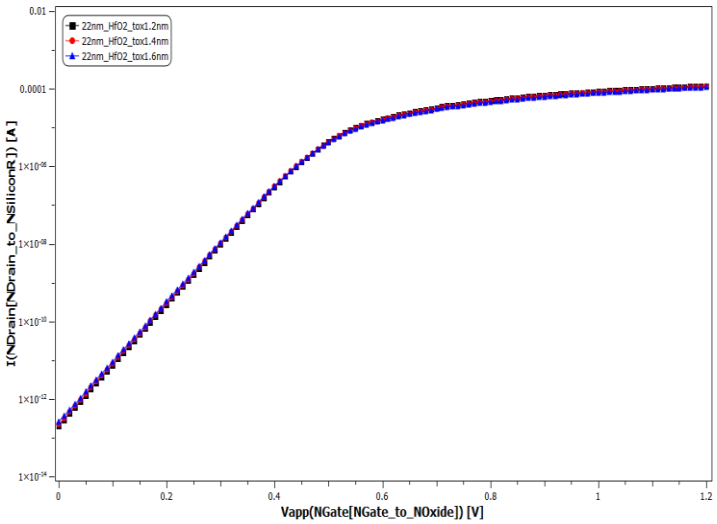
4.1.2 Id-Vgs characteristics for 22nm device using high k- dielectric

With 22nm high-k dielectric material, when doping concentration was varied the result show that in case of high doping concentration i.e. 1e19 the leakage current (approx 4.822e-15) is much reduced than that in low doping concentration i.e. 1e15 (approx 2.243e-13) as shown in figure 4.2(a) and figure 4.2(b) shows the variation of

drain current with respect to the gate voltage for different values of oxide thickness in which at the low oxide thickness i.e. 1.2nm the leakage current reduced much than that in high oxide thickness i.e. 1.6nm.



(a)



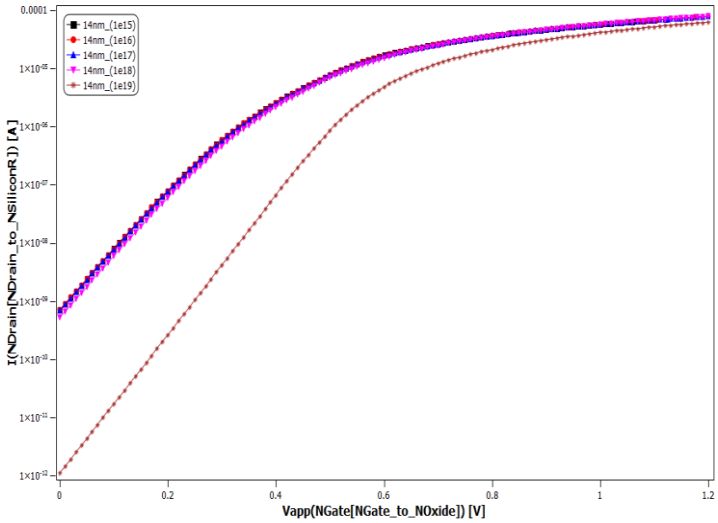
(b)

Fig. 4.2: Id-Vgs characteristics for high-k dielectric at 22nm for (a) different doping (b) different oxide thickness

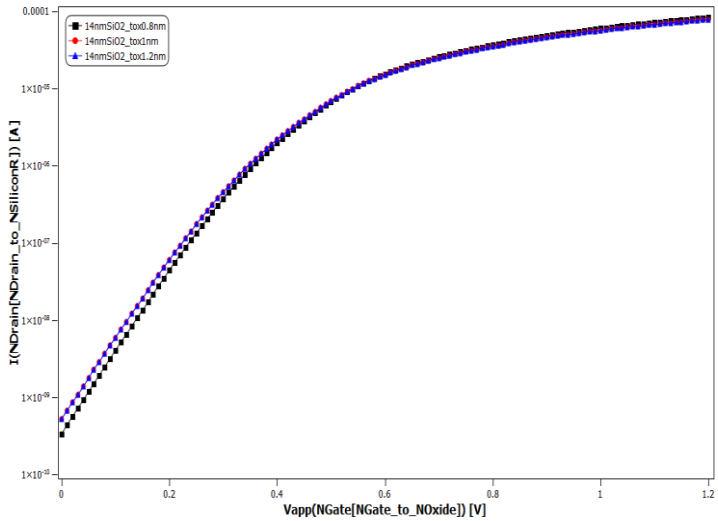
When the leakage current and drive current for both low-k dielectric and high-k dielectric material at 22nm technology node has compared it was found that leakage current has reduced more and drive current has increased more in high-k dielectric material than that in low-k dielectric material.

4.1.3 Id-Vgs characteristics for 14nm device using low k- dielectric

For 14nm low-k dielectric material, figure 4.3(a) illustrates the variation of drain current with respect to gate voltage for different values of doping concentration. The result show that in case of high doping concentration i.e. 1e19 the leakage current (approx 1.102e-12) is much reduced than that of low doping concentration i.e. 1e15 (approx 7.088e-10). Also, by the variation of oxide thickness it was observed that at low oxide thickness i.e. 0.8nm the value of leakage current was less than the current in high oxide thickness i.e. 1.2nm as depicted in figure 4.3(b)



(a)

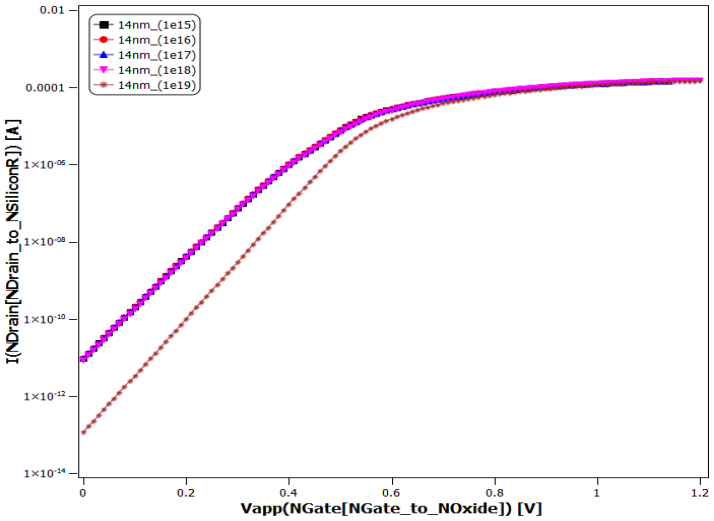


(b)

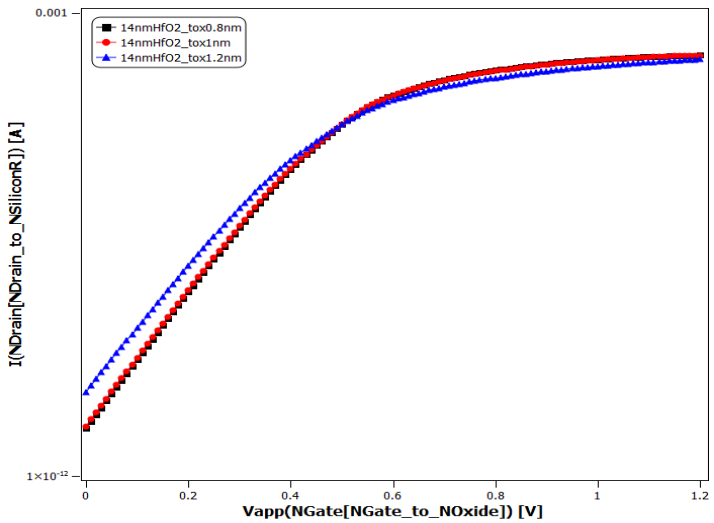
Fig. 4.3: Id-Vgs curve for low-k dielectric at 14nm for (a) different doping (b) different oxide thickness

4.1.4 Id-Vgs characteristics for 14nm device using high k- dielectric

With 14nm high-k dielectric material, doping concentration and oxide thickness was varied. The result show that in case of high doping concentration i.e. 1e19 the leakage current (approx 1.158e-13) is much reduced than that in low doping concentration i.e. 1e15 (approx 9.418e-12) as depicted in figure 4.4(a). Also, figure 4.4(b) illustrates the variation of oxide thickness in which low leakage current is obtained at the lower oxide thickness i.e. 0.8nm than that in 1.2nm.



(a)



(b)

Fig.4.4: Id-Vgs curve for low-k dielectric at 14nm for (a) different doping (b) different oxide thickness

When the leakage current and drive current for both low-k dielectric and high-k dielectric material at 14nm technology node has compared was found that leakage current has reduced more and drive current has increased more in high-k dielectric material than that in low-k dielectric material.

4.2 Study of various process parameters

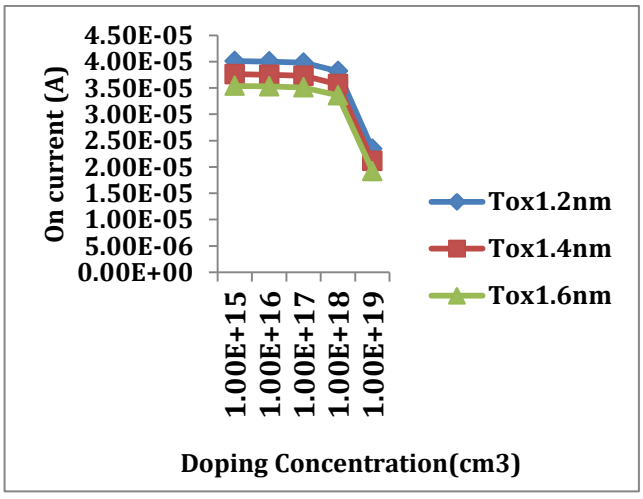
The study of various process parameters such as impact of doping concentration, fin height, fin width, underlap length and dielectric material have been done to analyze the device performance.

4.2.1 Impact of doping concentration

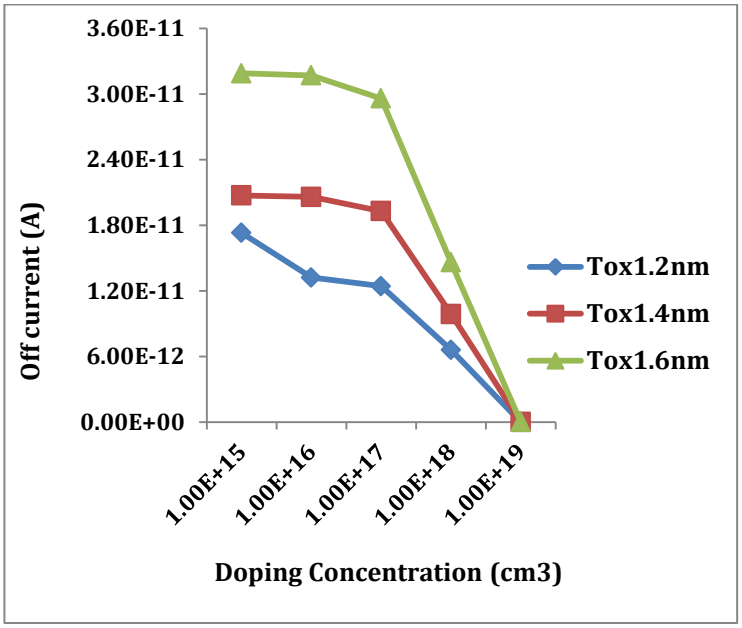
It was observed that as doping concentration increases, both drive current and leakage current get reduced and hence it led to the increment in on-off current ratio. As we move from low value of oxide thickness to high value of oxide thickness, over the different doping concentration, the lowest value of on current has been observed for the high value of oxide thickness and for the on-off current ratio the high value of oxide thickness shows the better results than other oxide thickness.

4.2.1.1 For low dielectric 22nm device

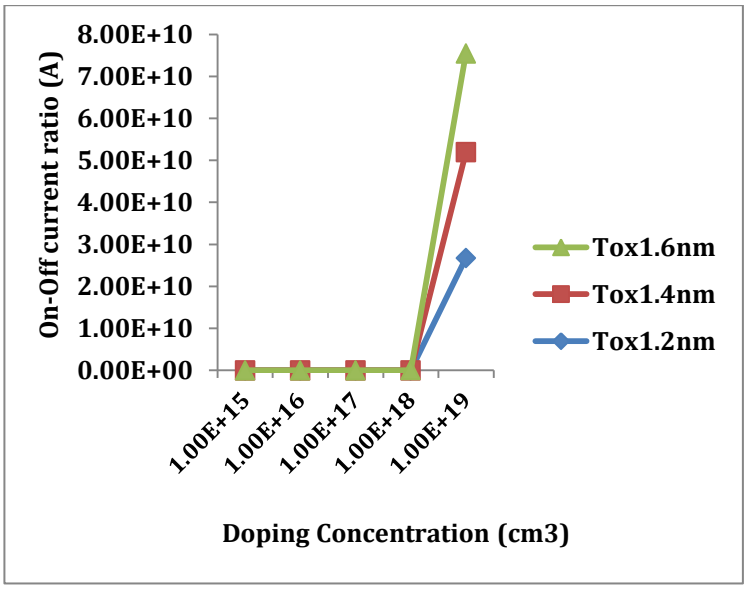
For different values of oxide thickness, as the doping concentration increases the inversion charge density decreases as a result threshold voltage increases that further leads to the linearly decrement in the value of drive current and exponentially decrement in the value of leakage current as shown in figure 4.5(a) and 4.5(b) respectively. By the figure 4.5(c) it is clear that the ratio of drive current to leakage current shows better performance when oxide thickness is 1.6nm. Also, when the doping concentration increases it leads to mobility degradation that further leads to increased capacitance due to which device scaling limits.



(a)



(b)



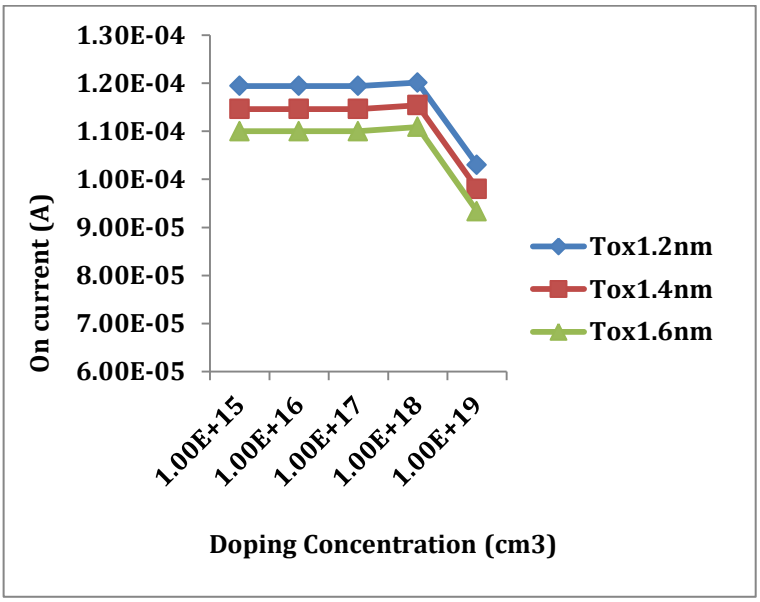
(c)

Fig. 4.5: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to different doping concentrations for low dielectric material at 22nm

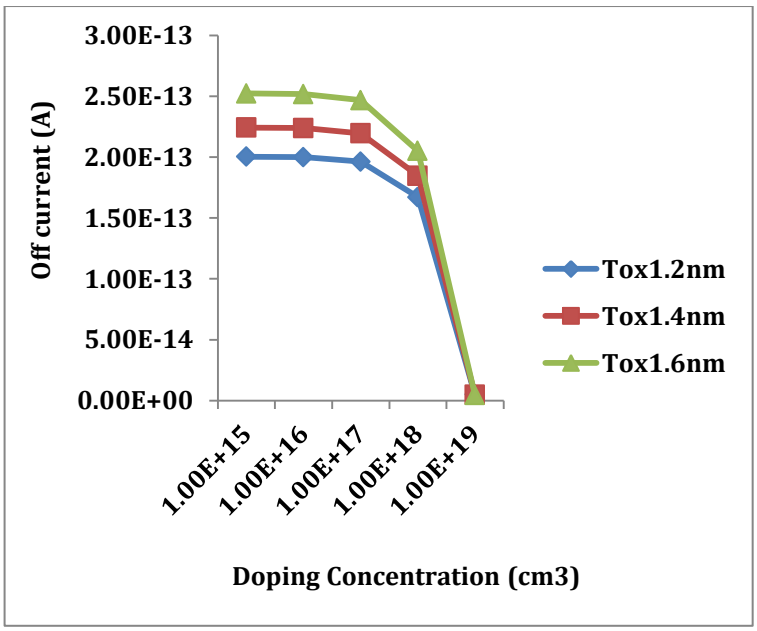
4.2.1.2 For high dielectric 22nm device

For 22nm technology node at high-k dielectric material, with the increase in doping concentration the value of drive current linearly decreases and leakage current exponentially decreases as shown in figure 4.6(a) and 4.6(b) respectively. The drive

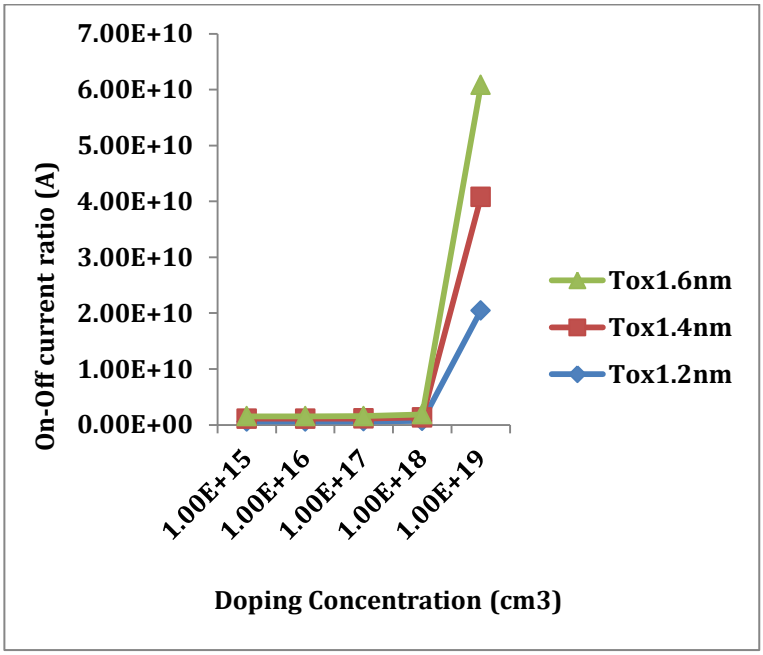
current for low doping concentration i.e. 1e15 varies from 1.19e-04, 1.15e-04 and 1.10e-04 to high doping concentration i.e. 1e19 from 1.03e-04, 9.80e-05 and 9.33e-05 and the leakage current for low doping concentration i.e. 1e15 varies from approx value of 2.00e-13, 2.24e-13 and 2.52e-13 to high doping concentration i.e. 1e19 in the range that approaches to zero (5.03e-15, 4.82e-15, 4.65e-15) for oxide thickness 1.2nm,1.4nm and 1.6nm respectively.



(a)



(b)

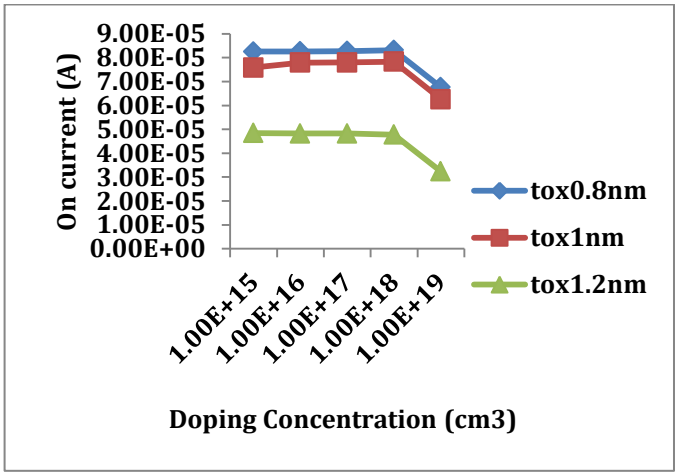


(c)

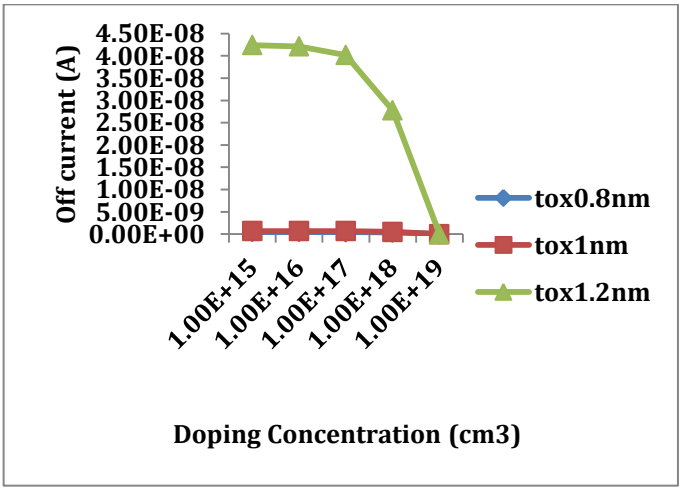
Fig. 4.6: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to different doping concentrations for high dielectric material at 22nm

4.2.1.3 For low dielectric 14nm device

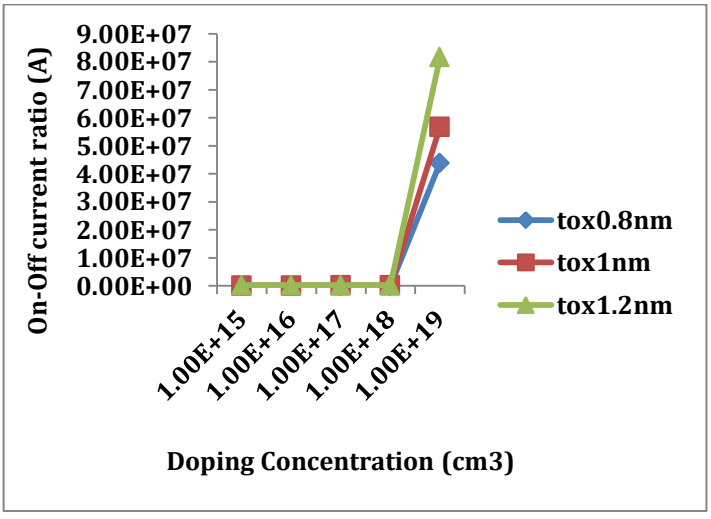
For 14nm technology node at low-k dielectric material, with the increase in doping concentration the value of drive current linearly decreases and leakage current exponentially decreases as shown in figure 4.7(a) and 4.7(b) respectively. The drive current for low doping concentration i.e. 1e15 varies from 8.10e-05, 7.50e-05 and 5.00e-05 to high doping concentration i.e. 1e19 from 6.50e-05, 6.00e-05 and 3.00e-05 and the leakage current for low doping concentration i.e. 1e15 varies from approx value of 4.00e-10, 7.00e-10 and 4.00e-08 to high doping concentration i.e. 1e19 in the range that approaches to zero (8.00e-13, 1.00e-12, 7.00e-13) for oxide thickness 0.8nm,1nm and 1.2nm respectively. By the figure 4.7(c) it is clear that the ratio of drive current to leakage current shows better performance when oxide thickness is 1.2nm as compared to other oxide thickness.



(a)



(b)

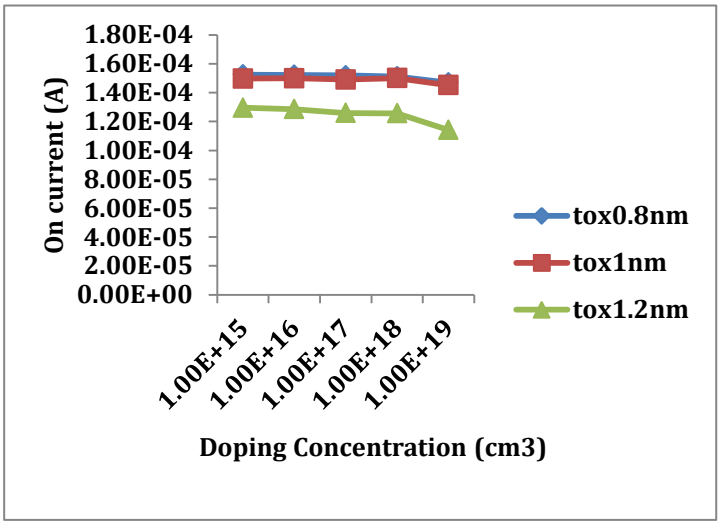


(c)

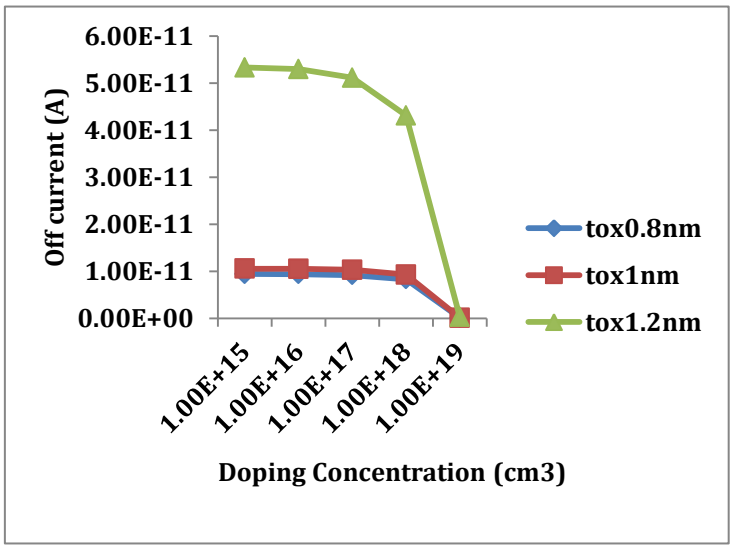
Fig. 4.7: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to different doping concentrations for low dielectric material at 14nm

4.2.1.4 For high dielectric 14nm device

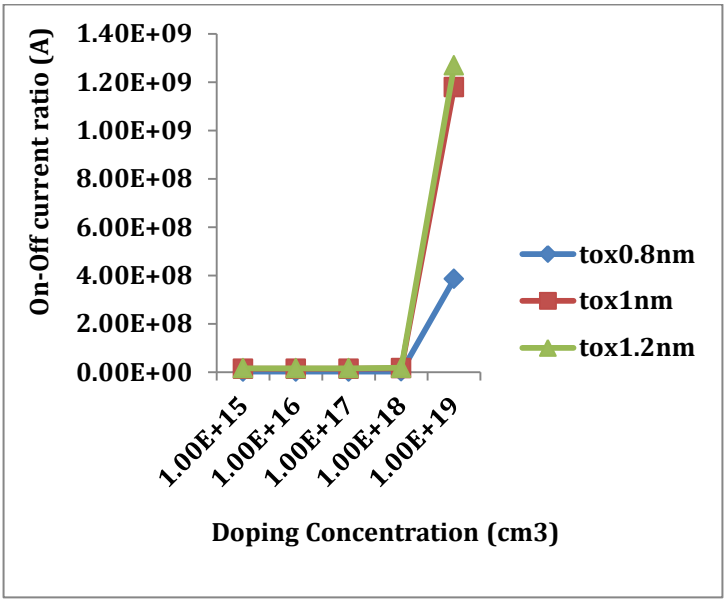
For different values of oxide thickness, as the doping concentration increases the inversion charge density decreases as a result threshold voltage increases that further leads to the linearly decrement in the value of drive current and exponentially decrement in the value of leakage current as shown in figure 4.8(a) and 4.8(b) respectively. For low doping concentration i.e. 1e15 the value of drive current varies from 1.53e-04, 1.50e-04 and 1.30e-04 to high doping concentration i.e. 1e19 from 1.47e-04, 1.45e-04 and 1.14e-04 and leakage current varies from approx value of 9.42e-12, 1.06e-11 and 5.33e-11 to high doping concentration i.e. 1e19 in the range that approaches to zero (1.16e-13, 1.23e-13, 2.96e-13) for oxide thickness 0.8nm, 1nm and 1.2nm respectively. By the figure 4.8(c) it is clear that the ratio of drive current to leakage current shows better performance when oxide thickness is 1.2nm.



(a)



(b)



(c)

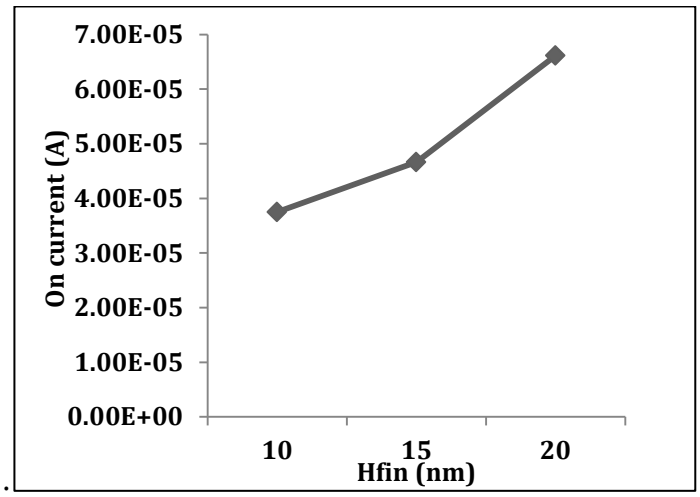
Fig. 4.8: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to different doping concentrations for high dielectric material at 14nm

4.2.2 Impact of Fin Height

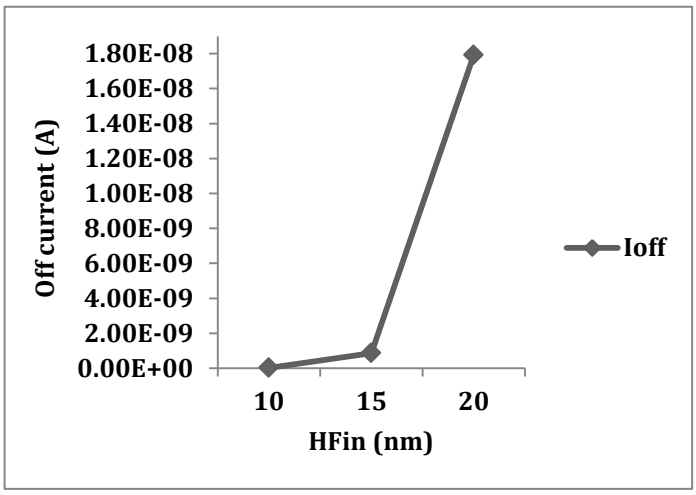
It was observed that as the height of fin increases the drive current of the device increases because of the increase in channel inversion area and the leakage current increases because of the decrement in gate supremacy of the channel and hence the on-off current ratio decreased.

4.2.2.1 For low dielectric 22nm device

With the increase in fin height from 10nm to 20nm because of the increment in channel inversion area of the device the drive current of the device increases and the leakage current of the device increases due to the decrement in gate supremacy of the channel as shown in figure 4.9(a) and 4.9(b) respectively. The figure 4.9(c) shows that at fin height 10nm the ratio of on-off current is much more than other increasing fin height. Less will be the value of fin height better will be the performance of device.



(a)



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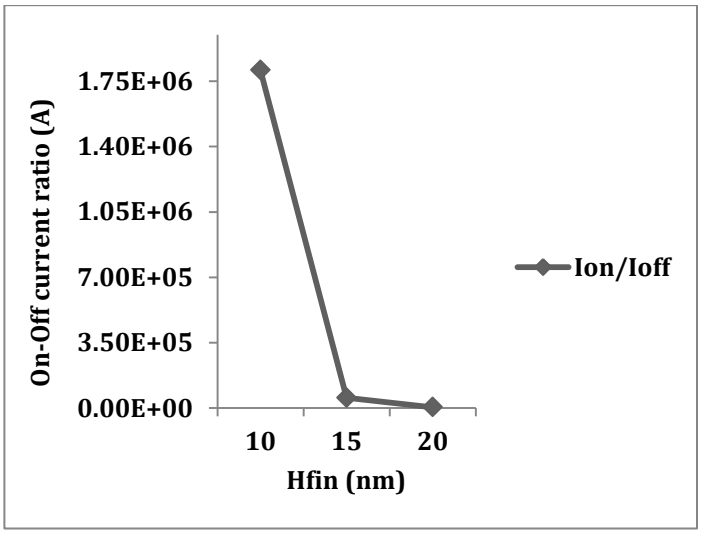
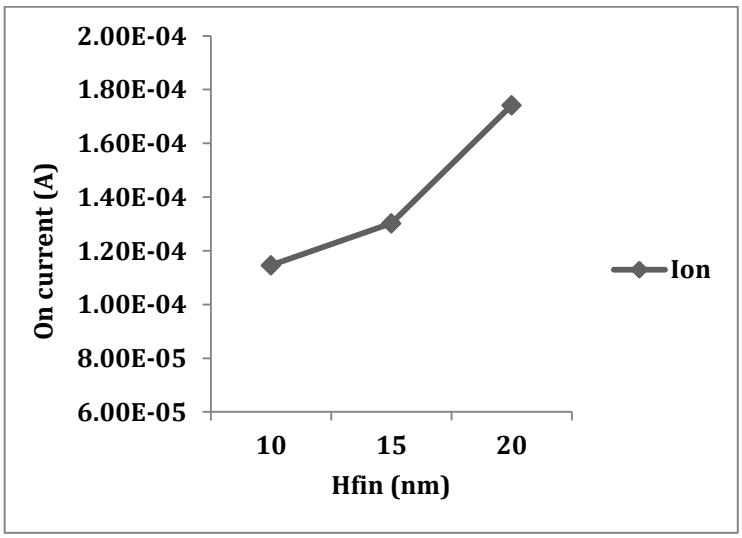


(c)

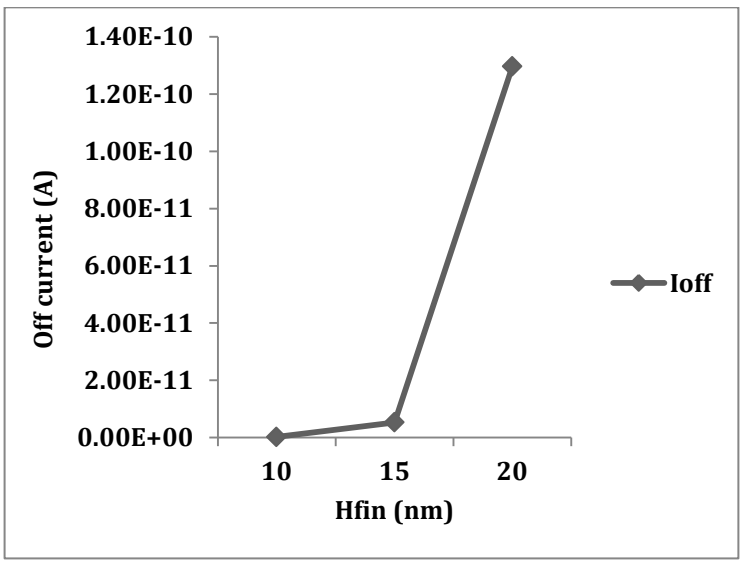
Fig.4.9: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin height variation for low dielectric material at 22nm.

4.2.2.2 For high dielectric 22nm device

For 22nm device with high dielectric, as the height of fin increases from 10nm to 20 nm the drive current of the device varies from approx value 1.15e-04 to1.74e-04 because of the increment in channel inversion area and leakage current varies from 2.24e-13 to 1.30e-10 due to the decrement in gate supremacy of the channel as shown in figure 4.10(a) and 4.10(b) respectively. By the figure 4.10(c) it is clear that at fin height 10nm the ratio of on-off current is much more than other increasing fin heights.



(a)



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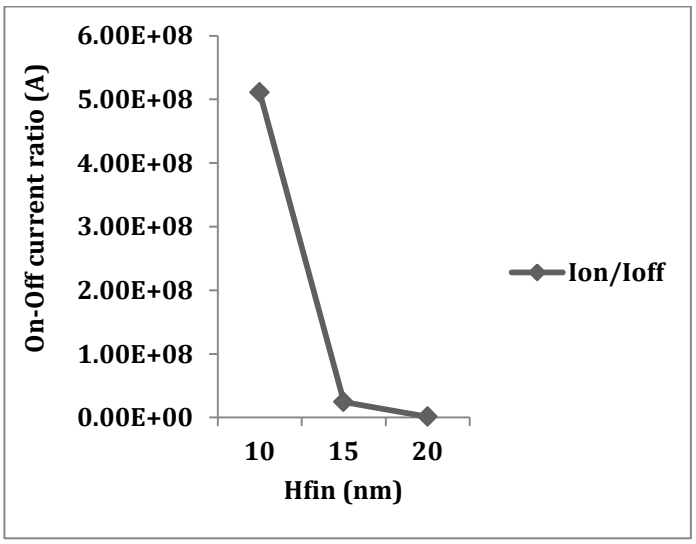
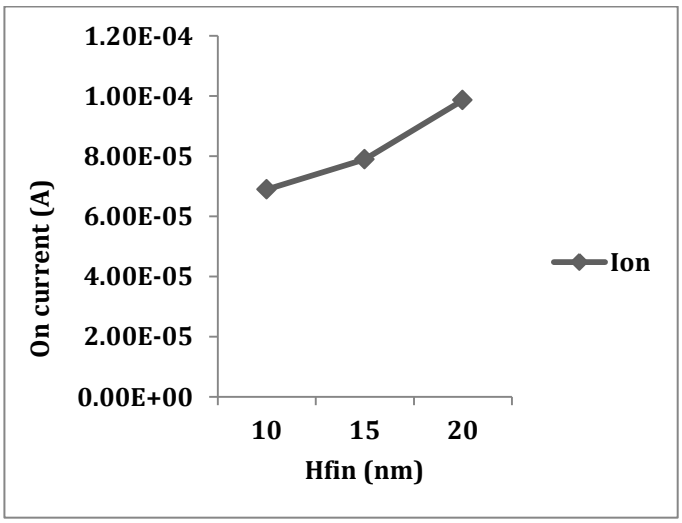


(c)

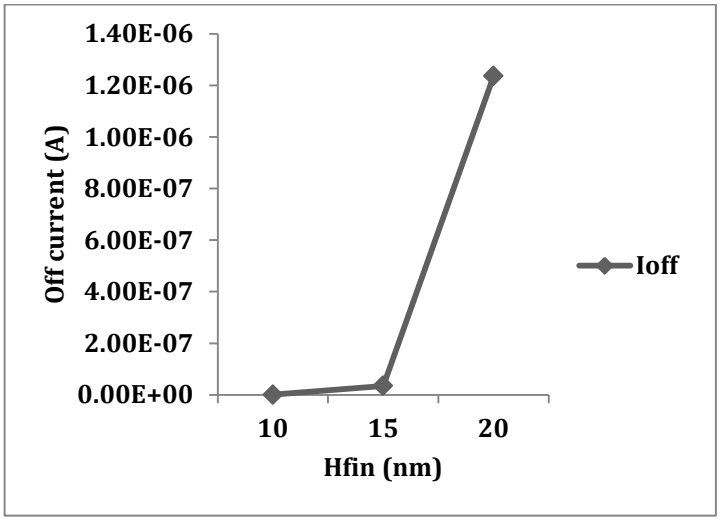
Fig.4.10: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin height variation for high dielectric material at 22nm.

4.2.2.3 For low dielectric 14nm device

For 14nm device with low dielectric, as the height of fin increases from 10nm to 20 nm the drive current of the device varies from approx value 6.89e-05 to 9.86e-05 because of the increment in channel inversion area and leakage current varies from 4.67e-10 to 1.24e-06 due to the decrement in gate supremacy of the channel as shown in figure 4.11(a) and 4.11(b) respectively. By the figure 4.11(c) it is clear that at fin height 10nm the ratio of on-off current is much more than other increasing fin heights. Hence the less value of fin height is desired.



(a)



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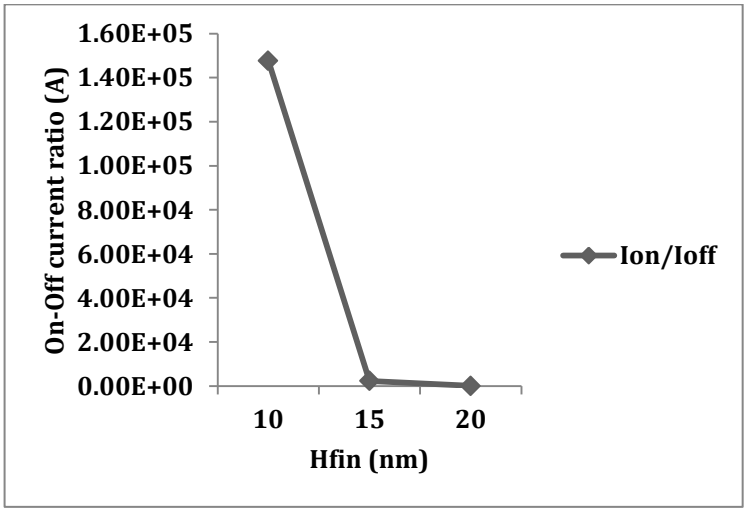
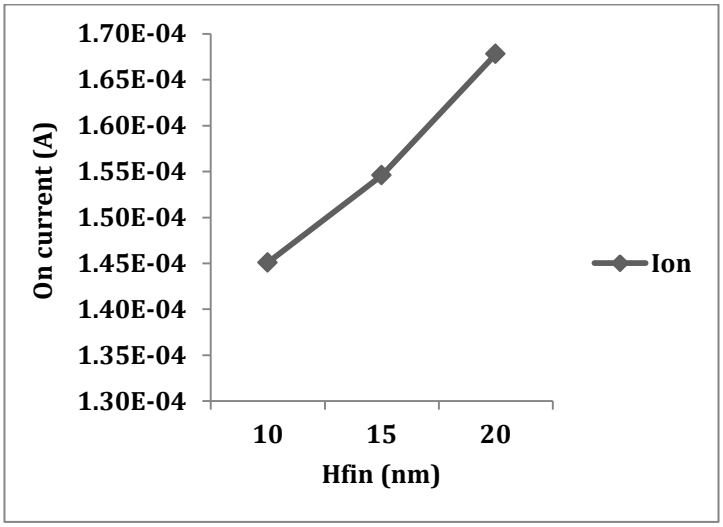


(c)

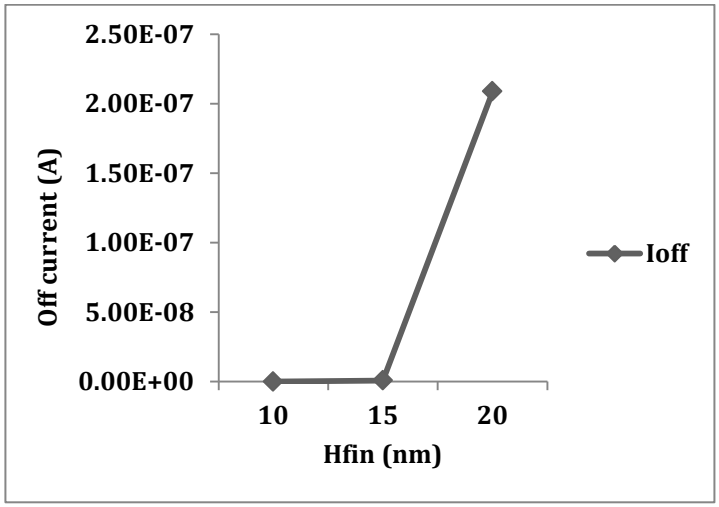
Fig.4.11: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin height variation for low dielectric material at 14nm.

4.2.2.4 For high dielectric 14nm device

With the increase in fin height from 10nm to 20nm because of the increment in channel inversion area of the device the drive current of the device increases from approx value 1.45e-04 to 1.68e-04 and the leakage current of the device increases due to the decrement in gate supremacy of the channel from approx value nearby zero i.e. 9.42e-13 to 2.09e-07 as shown in figure 4.12(a) and 4.12(b) respectively. The figure 4.12(c) shows that at fin height 10nm the ratio of on-off current is much more than other increasing fin height. Less will be the value of fin height better will be the performance of device.



(a)



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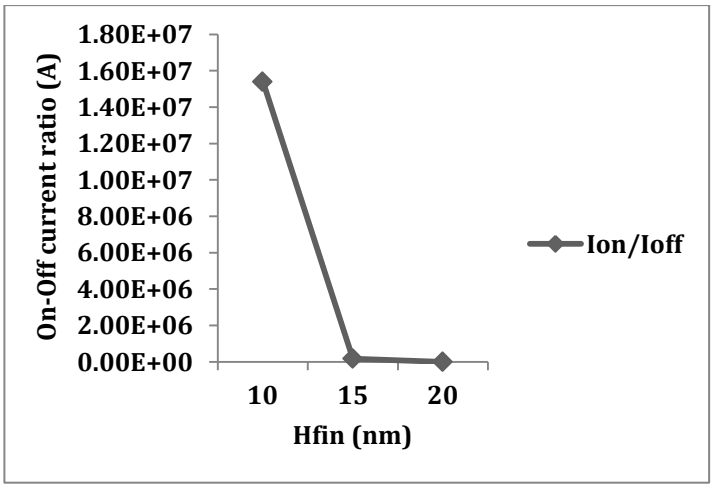


(c)

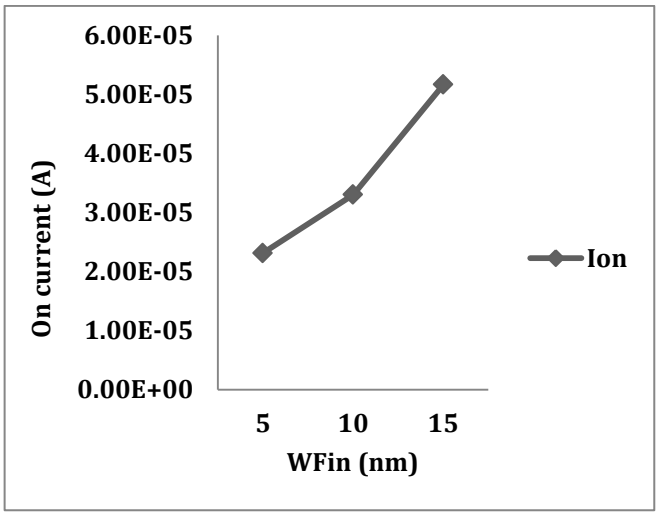
Fig.4.12: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin height variation for high dielectric material at 14nm.

4.2.3 Impact of Fin Width

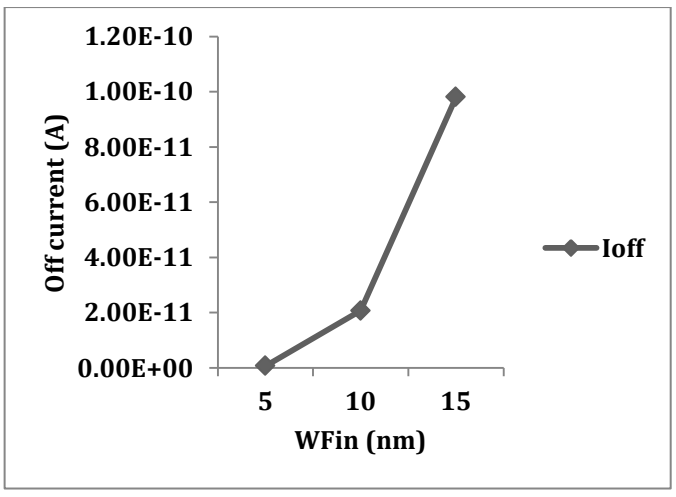
It was observed that as the width of fin increases the drive current of the device increases because of the increment in channel inversion area and the leakage current increases because of the decrement in gate supremacy of the channel and hence the on-off current ratio decreased.

4.2.3.1 For low dielectric 22nm device

For 22nm device with low dielectric, as the fin width increases from 5nm to 15 nm the drive current of the device varies from approx value 2.31e-05 to 5.17e-05 because of the increment in channel inversion area and leakage current varies from 7.23e-13 to 9.81e-11 due to the decrement in gate supremacy of the channel as shown in figure 4.13(a) and 4.13(b) respectively. By the figure 4.13(c) it is clear that at fin width 5nm the ratio of on-off current is much more than other increasing fin widths. Hence less value of fin width is desired.



(a)



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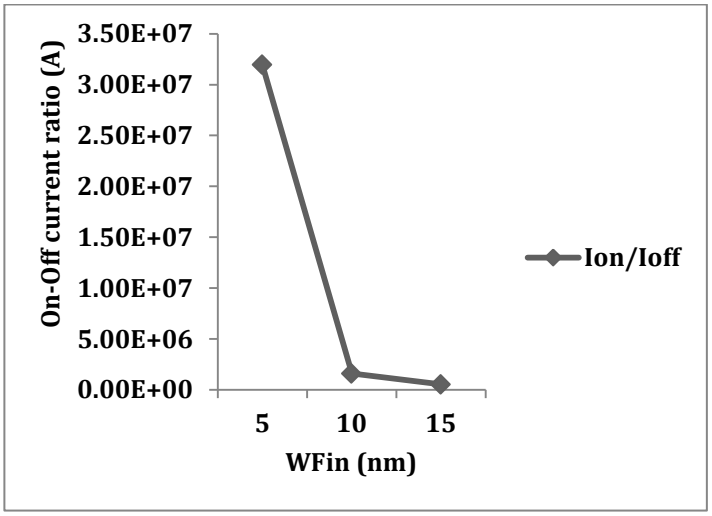
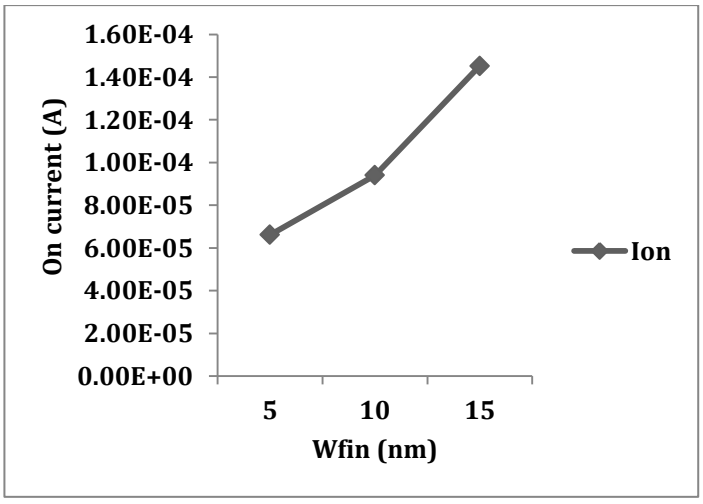


(c)

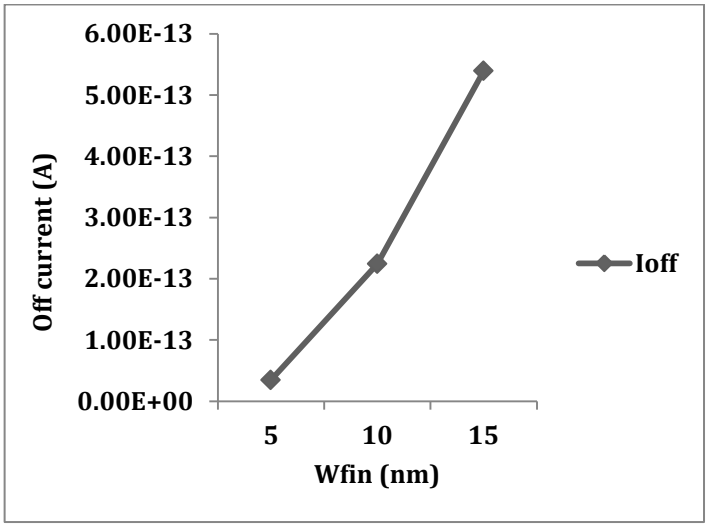
Fig.4.13: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin width variation for low dielectric material at 22nm.

4.2.3.2 For high dielectric 22nm device

With the increase in width of fin from 5nm to 15nm because of the increment in channel inversion area of the device the drive current of the device increases from 6.62e-05 to 1.45e-04 and the leakage current of the device increases due to the decrement in gate supremacy of the channel from 3.48e-14 to 5.40e-13 as shown in figure 4.14(a) and 4.14(b) respectively. The figure 4.14(c) shows that at fin width 5nm the ratio of on-off current is much more than other increasing fin width. Less will be the value of fin width better will be the performance of device.



(a)



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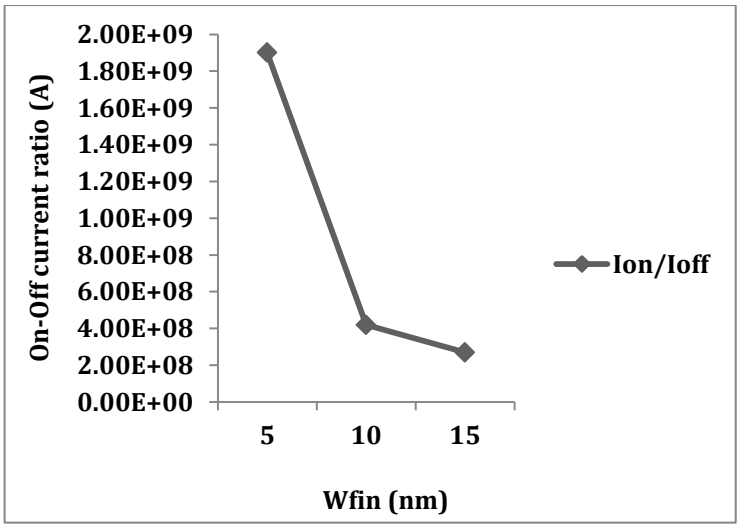
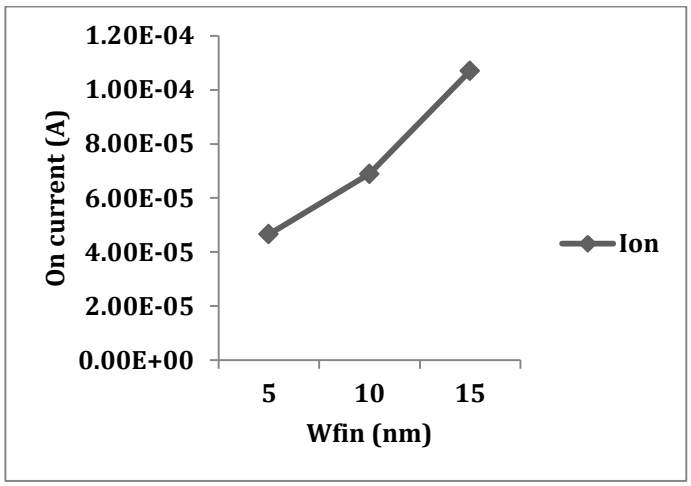


(c)

Fig.4.14: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin width variation for high dielectric material at 22nm.

4.2.3.3 For low dielectric 14nm device

With the increase in fin width from 5nm to 15nm because of the increment in channel inversion area of the device the drive current of the device increases from approx value 4.66e-05 to 1.07e-04 and the leakage current of the device increases due to the decrement in gate supremacy of the channel from approx value nearby zero i.e. 3.31e-12 to 2.81e-09 as shown in figure 4.15(a) and 4.15(b) respectively. The figure 4.15(c) shows that at fin width 5nm the ratio of on-off current is much more than other increasing fin width. Less will be the value of fin width better will be the performance of device.



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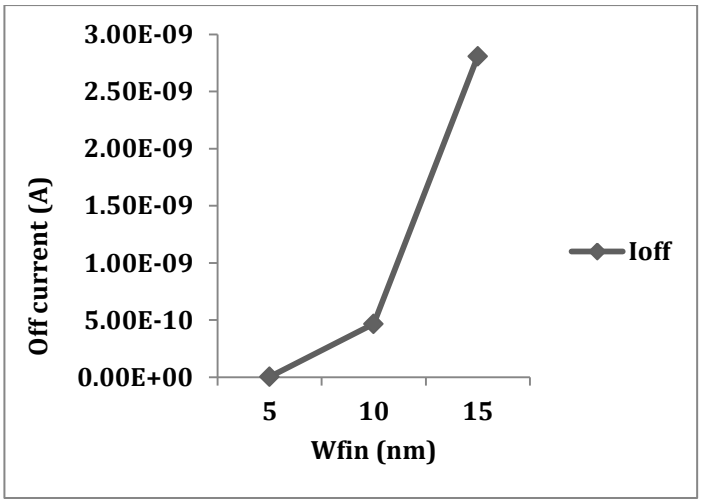

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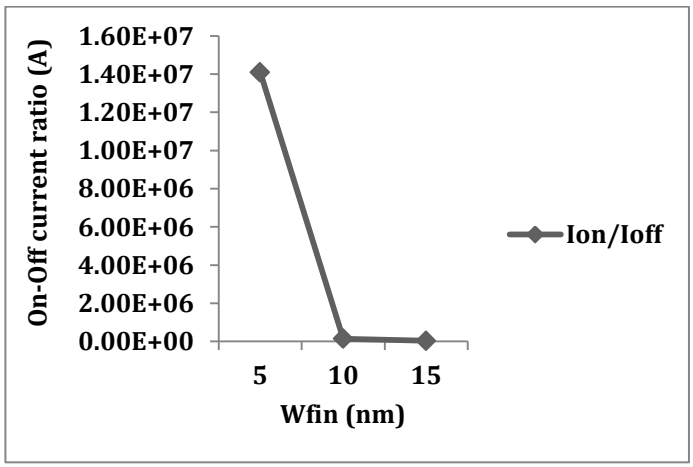
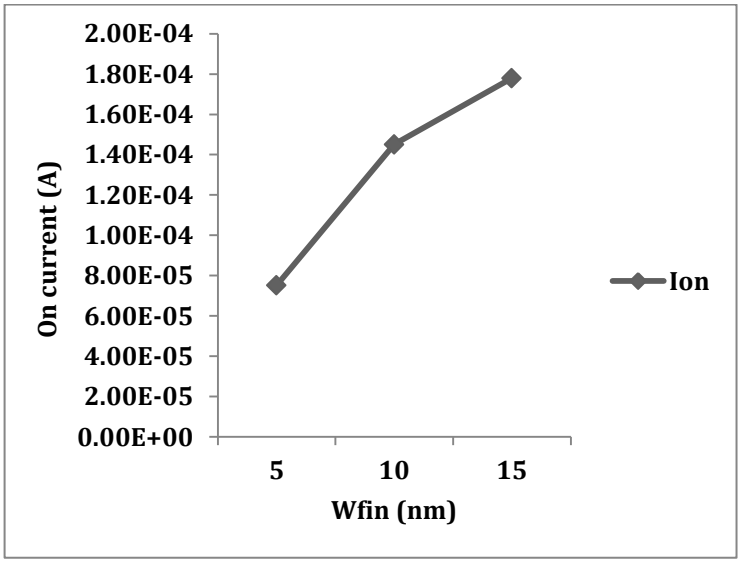


(c)

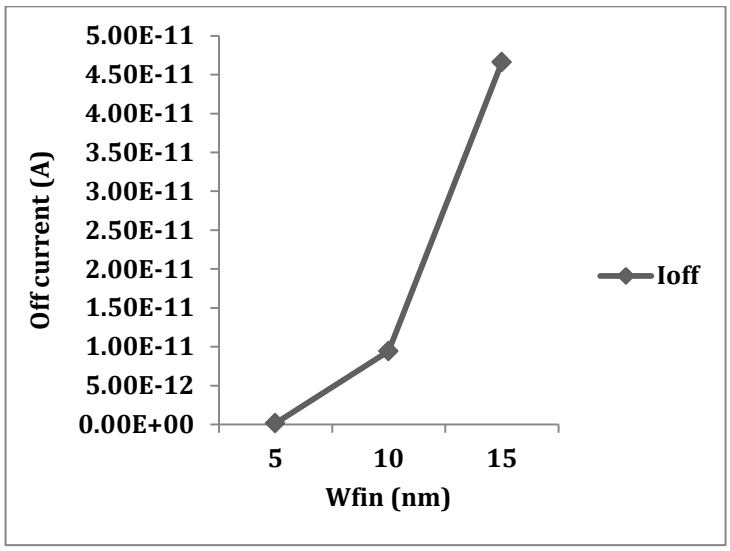
Fig.4.15: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin width variation for low dielectric material at 14nm.

4.2.3.4 For high dielectric 14nm device

For 14nm device with high dielectric, as the fin width increases from 5nm to 15 nm the drive current of the device varies from approx value 7.52e-05 to 1.78e-04 because of the increment in channel inversion area and leakage current varies from 1.62e-13 to 4.66e-11 due to the decrement in gate supremacy of the channel as shown in figure 4.16(a) and 4.16(b) respectively. By the figure 4.16(c) it is clear that at fin width 5nm the ratio of on-off current is much more than other increasing fin widths. Hence less value of fin width is desired.



(a)



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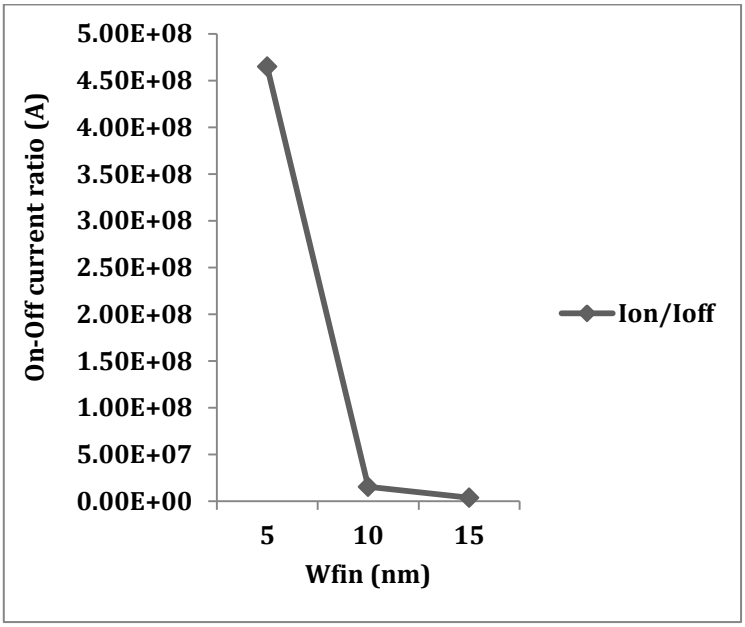


(c)

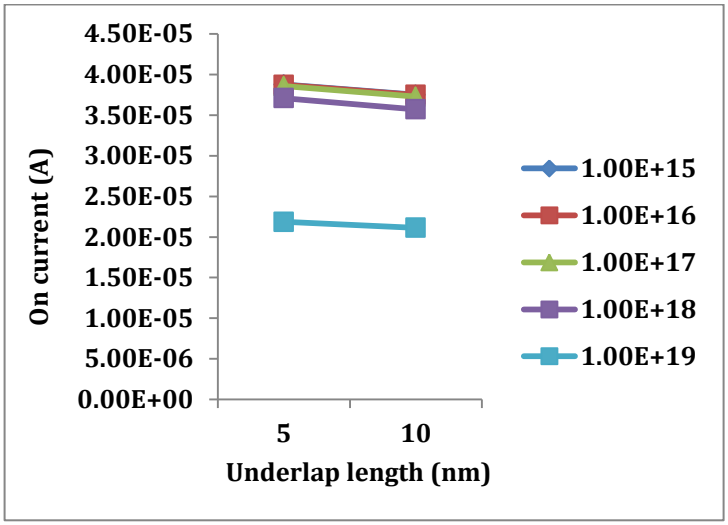
Fig.4.16: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to fin width variation for high dielectric material at 14nm.

4.2.4 Impact of Underlap length

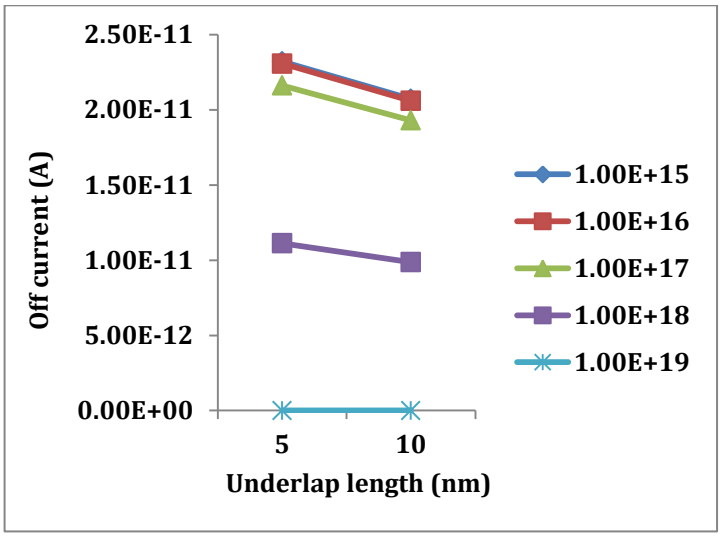
It was observed that as the length of underlap increases, both drive current and leakage current decrease resulting in the increment of on-off current ratio and improvement in device performance.

4.2.4.1 For low dielectric 22nm device

With the increment in underlap length of 22nm low-k dielectric device the distance between source and drain increases due to which resistance between source and drain terminal increased that further leads to decrement in gate oxide capacitance resulting in decrement in drive current as shown in figure 4.17(a). With the increase in barrier height charge carrier faces problem in tunnelling from source to drain due to which drain influence on channel region reduces. That leads to decrement in leakage current as shown in figure 4.17(b). Figure 4.17(c) illustrates that the on-off current ratio increased at high underlap length having the high doping concentration i.e. 1e19.



(a)



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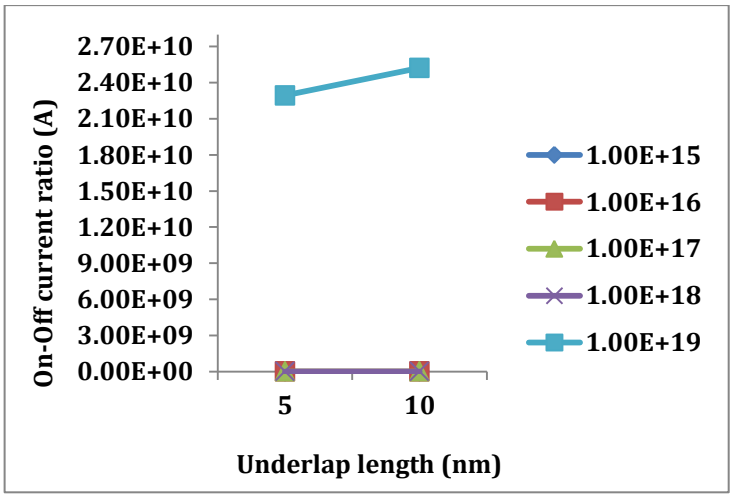
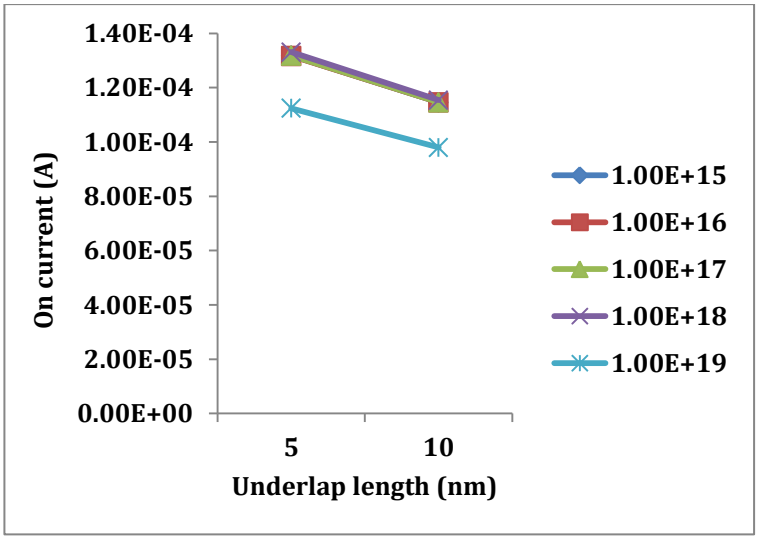


(c)

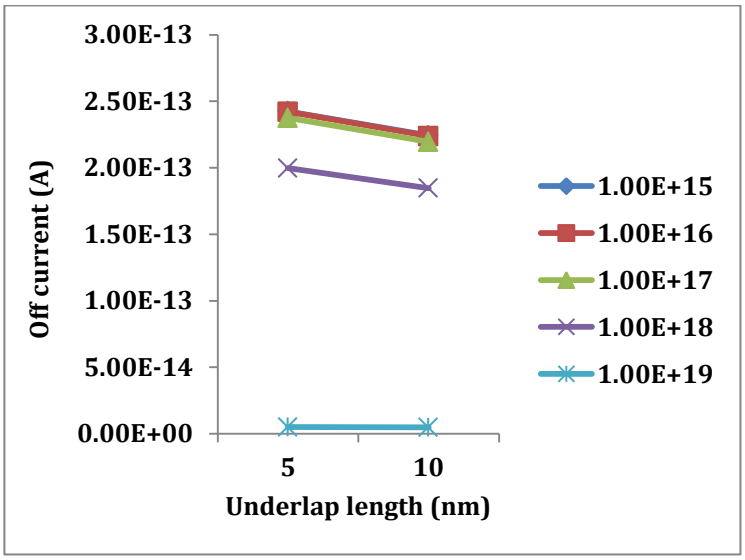
Fig.4.17: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to underlap length for low dielectric material at 22nm.

4.2.4.2 For high dielectric 22nm device

For 22nm device with high-k dielectric material as the underlap length increases it leads to increment in the resistance between source and drain that leads to the decrement in drive current and leakage current as shown in figure 4.18(a) 4.18(b) respectively. The use of high-k dielectric material increases the fringing field that causes the barrier lowering hence more carrier enter from source to drain resulting in higher drive current as comparison to low-k dielectric material. The figure 4.18(c) illustrates that for different values of doping concentration, as the length of underlap increases the ratio of on-off current increased at high underlap length having the high doping concentration i.e. 1e19.



(a)



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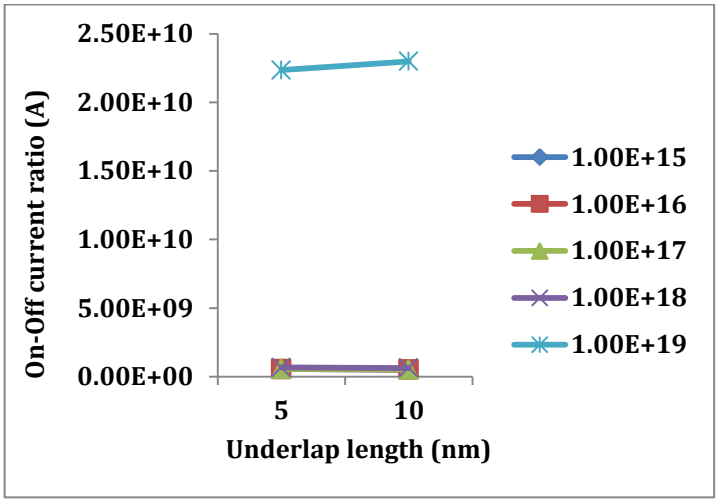
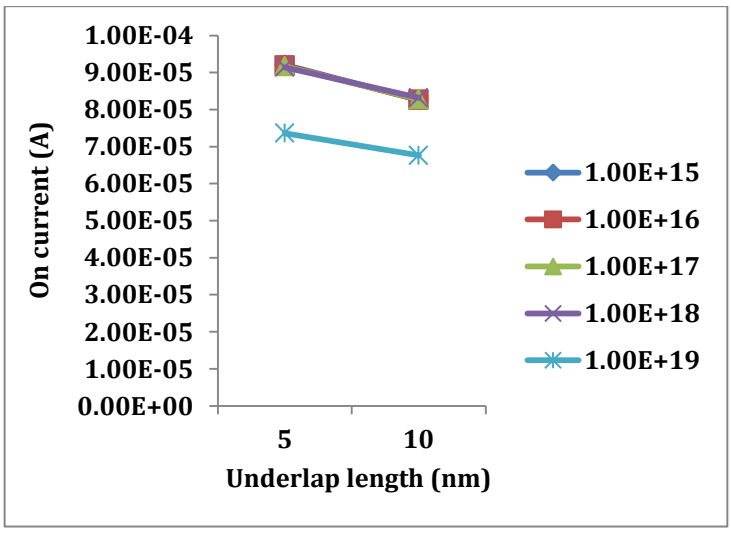


(c)

Fig.4.18: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to underlap length for high dielectric material at 22nm.

4.2.4.3 For low dielectric 14nm device

In case of 14nm technology node with low-k dielectric material as the length of underlap increases, distance between source and drain increases due to which resistance between source and drain terminal increased that further leads to decrement in gate oxide capacitance resulting in decrement in drive current as shown in figure 4.19(a). With the increase in barrier height charge carrier faces problem in tunnelling from source to drain due to which drain influence on channel region reduces. That leads to decrement in leakage current as shown in figure 4.19(b). By the figure 4.19(c) it is clear that for different values of doping concentration, as the length of underlap increases the ratio of on-off current increased at high underlap length having the high doping concentration i.e. 1e19.



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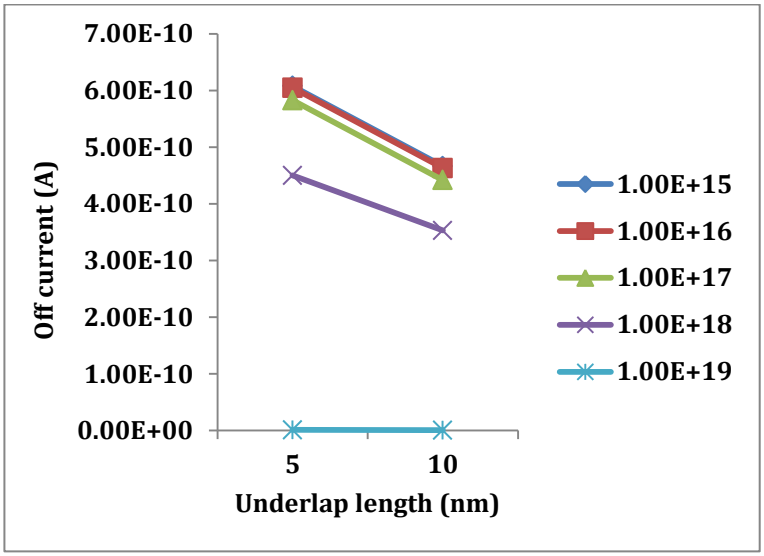

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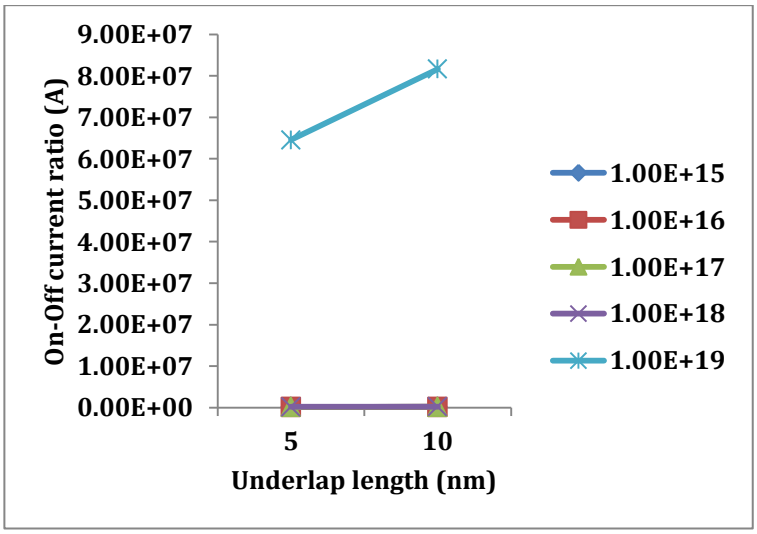
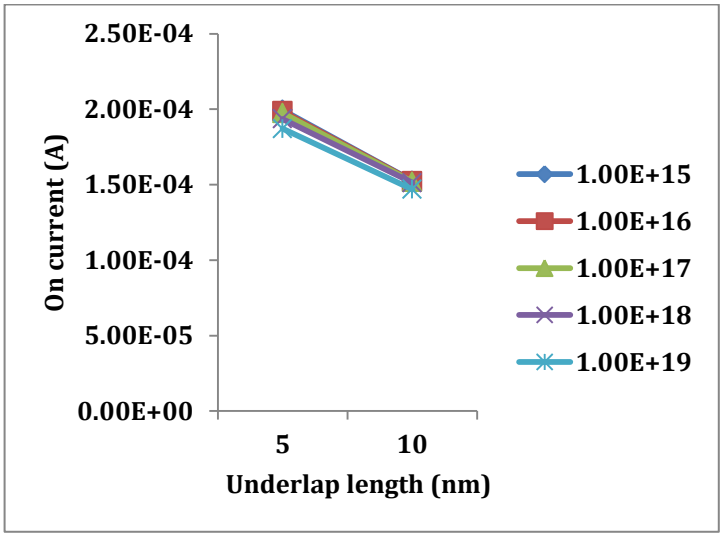


(c)

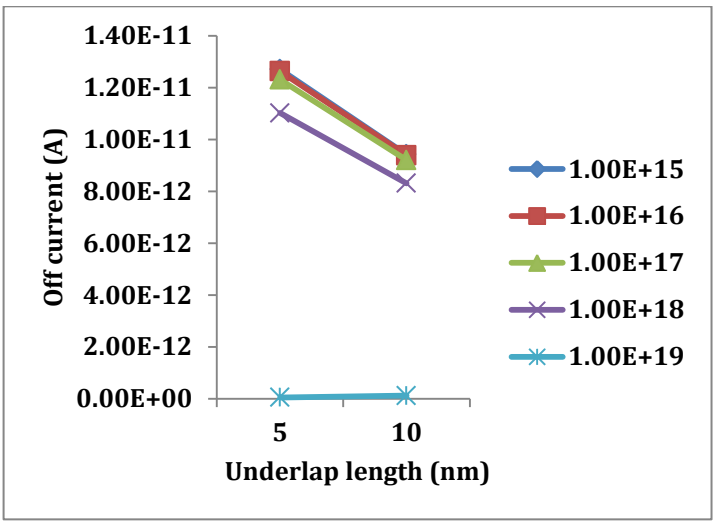
Fig.4.19: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to underlap length for low dielectric material at 14nm.

4.2.4.4 For high dielectric 14nm device

In the figure 4.20(a) and 4.20(b) shown below, it is clear that increasing the underlap length leads to increment in the resistance between source and drain that leads to the decrement in drive current and leakage current respectively. By the figure 4.19(c) it is clear that for different values of doping concentration, as the length of underlap increases the ratio of on-off current decreased at high underlap length having the high doping concentration i.e. 1e19.



(a)



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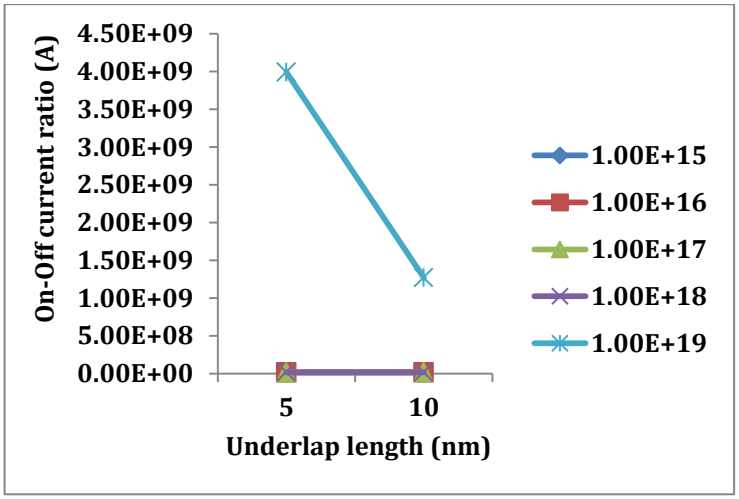


(c)

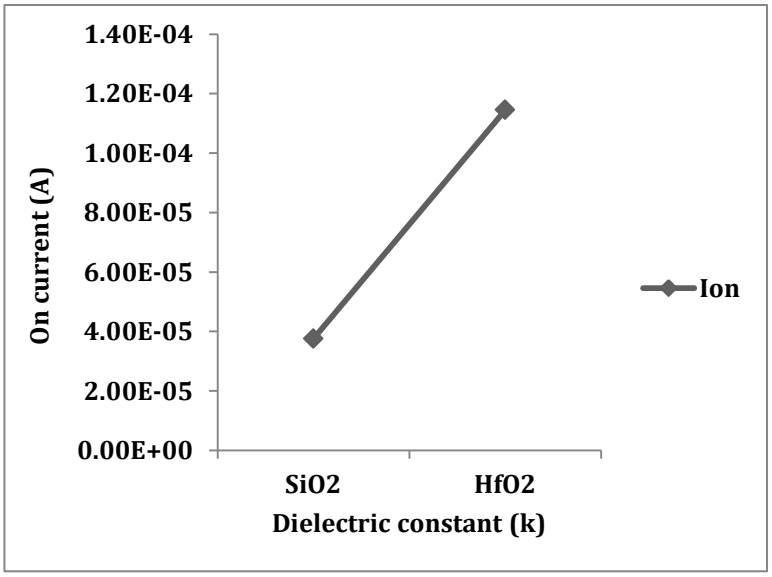
Fig.4.20: Variation of (a) drive current (b) leakage current (c) on-off current ratio with respect to underlap length for high dielectric material at 14nm.

4.2.5 Impact of Dielectric material

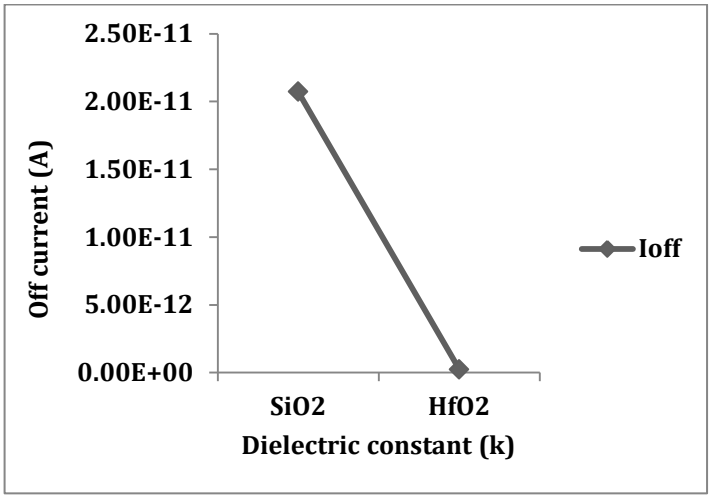
With the use of high k- dielectric the drive current of device increases, since the fringing field increases that causes the barrier lowering in underlap regions. Hence the performance of device at high k-dielectric material increased than that in low k-dielectric material device.

4.2.5.1 For 22nm device

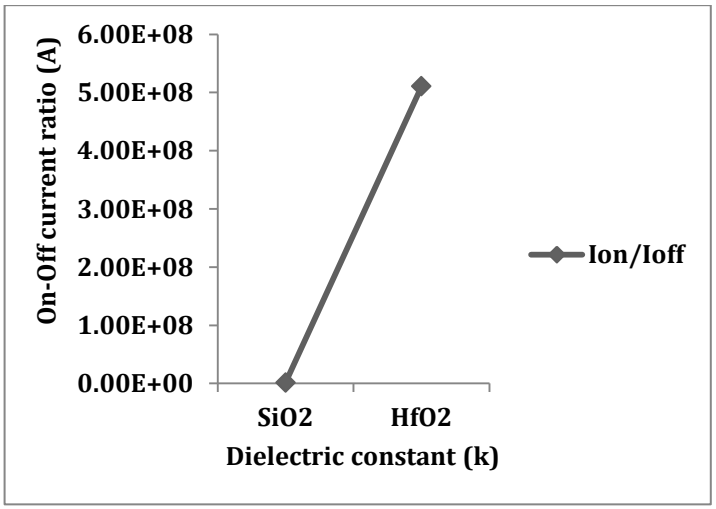
When the drive current for low-k dielectric and high-k dielectric material is compared it was found that for low-k dielectric i.e. SiO2 the value of current is approx 3.76-05 whereas for high-k dielectric material i.e. HfO2 the value of current is approx 1.15e-04, which is very high in comparison to low-k dielectric material as shown in figure 4.21(a). Replacing SiO2 with HfO2 improved the oxide capacitance as a result leakage current reduced from approx value of 2.07e-11 to 2.24e-13 which will give better stability and low power consumption as shown in figure 4.21(b). The figure 4.21(d) and 4.21(e) shown below illustrates the less value of DIBL and SS respectively in case of high-k dielectric material than that in low-k dielectric material.



(a)


2.50E-11
2.00E-11
1.50E-11
1.00E-11
5.00E-12
0.00E+00
Off current (A)
SiO2
HfO2
Dielectric constant (k)
Ioff

(b)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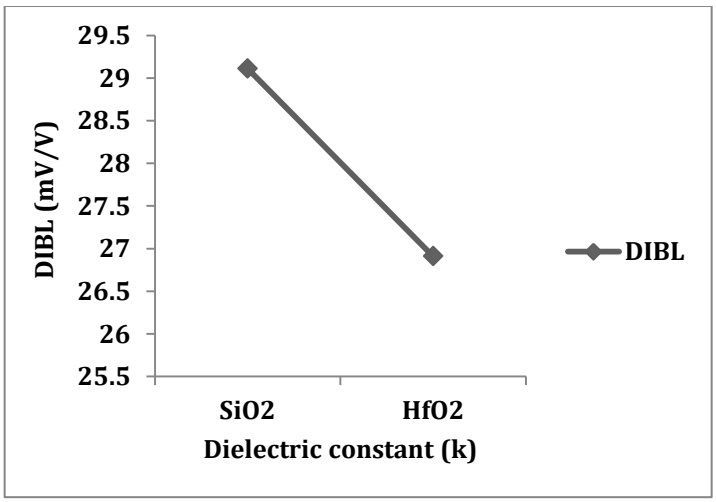
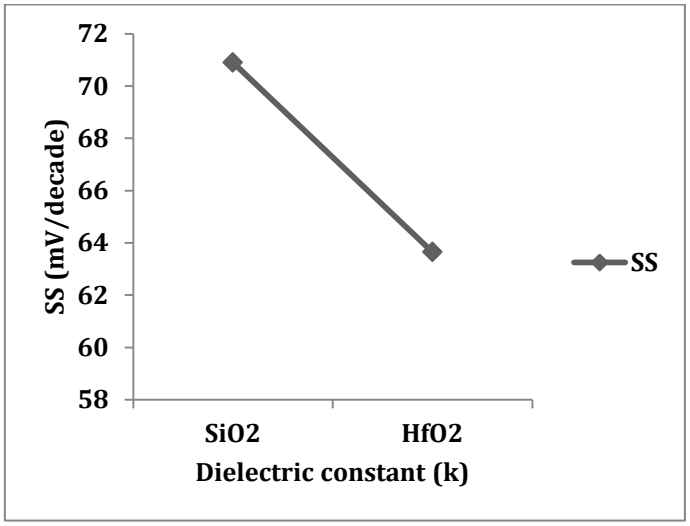
5.00E+08
4.00E+08
3.00E+08
2.00E+08
1.00E+08
0.00E+00
On-Off current ratio (A)
SiO2
HfO2
Dielectric constant (k)
Ion/Ioff

(c)


29.5
29
28.5
28
27.5
27
26.5
26
25.5
DIBL (mV/V)
SiO2
HfO2
Dielectric constant (k)
DIBL

(d)

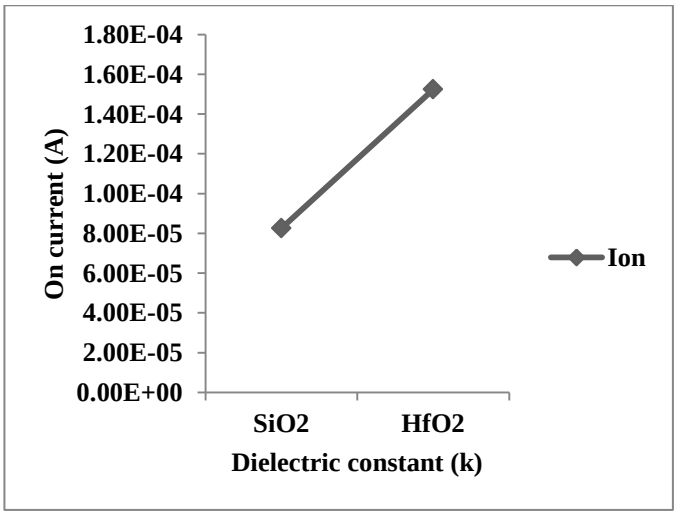


(e)

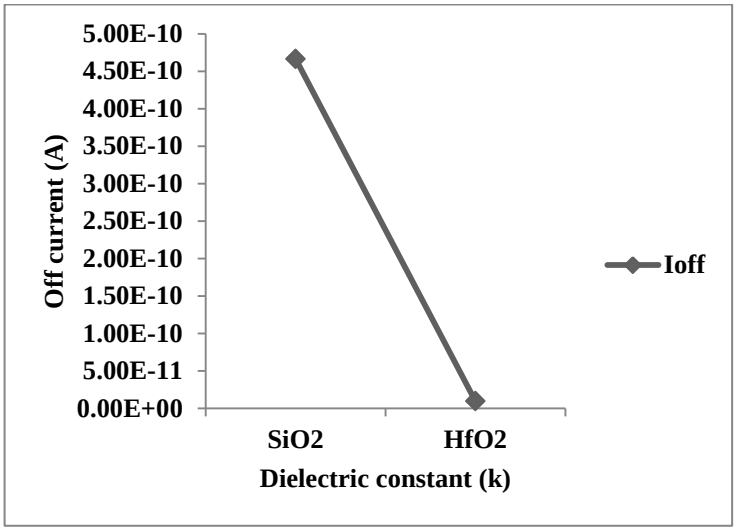
Fig.4.21: Variation of (a) drive current (b) leakage current (c) on-off current ratio (d) DIBL (e) SS with respect to dielectric materials at 22nm.

4.2.5.2 For 14nm device

When the drive current for low-k dielectric and high-k dielectric material is compared it was found that for low-k dielectric i.e. SiO2 the value of current is approx 8.26e-05 whereas for high-k dielectric material i.e. HfO2 the value of current is approx 1.53e-04 as shown in figure 4.22(a), which is very high in comparison to low-k dielectric material. The leakage current varies from 4.67e-10 to 9.42e-12 in low-k to high-k material respectively as shown in figure 4.22(b). The figure 4.22(d) and 4.22(e) shown below illustrates the reduced DIBL and SS values respectively in case of high-k dielectric material than that in low-k dielectric material.



(a)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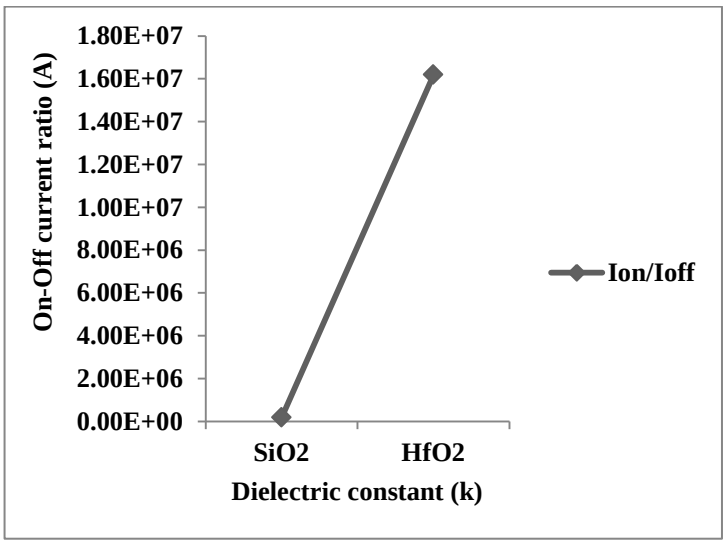
1.50E-10
1.00E-10
5.00E-11
0.00E+00
Off current (A)
SiO2
HfO2
Dielectric constant (k)
Ioff

(b)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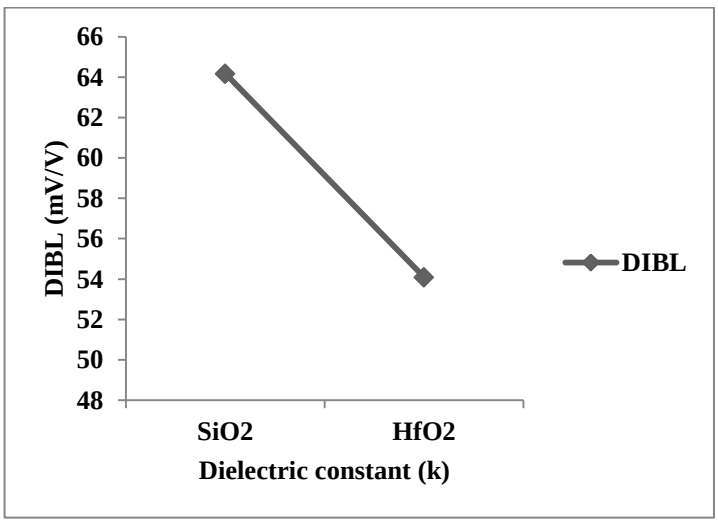
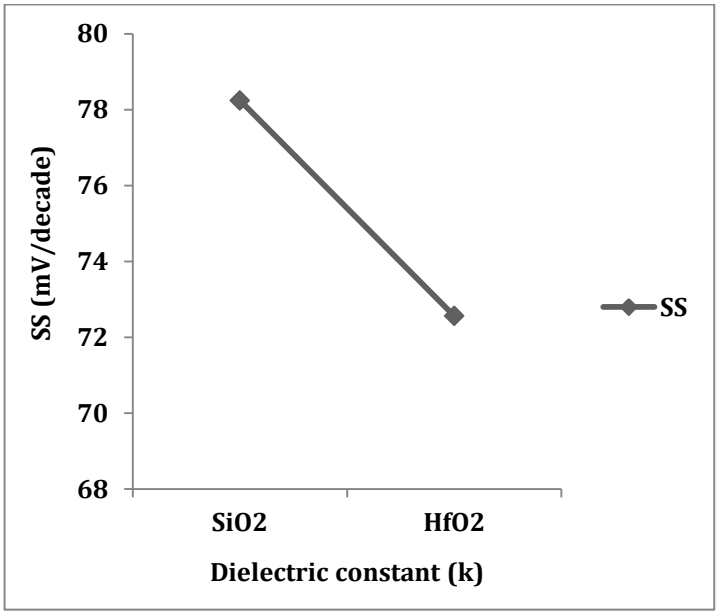
8.00E+06
6.00E+06
4.00E+06
2.00E+06
0.00E+00
On-Off current ratio (A)
SiO2
HfO2
Dielectric constant (k)
Ion/Ioff

(c)


66
64
62
60
58
56
54
52
50
48
DIBL (mV/V)
SiO2
HfO2
Dielectric constant (k)
DIBL

(d)



(e)

Fig.4.22: Variation of (a) drive current (b) leakage current (c) on-off current ratio (d) DIBL (e) SS with respect to dielectric materials at 14nm.

After analyzing the best performance of device at different process parameters we have performed a simulation by taking all the parameters that are minimum height of fin as 10nm, minimum width of fin as 5nm, maximum doping concentration as 1e19 and minimum oxide thickness as 1.2nm and 0.8nm for 22nm and 14nm respectively. The values obtained after the simulation is shown in the table 4.1 and 4.2 below:

Table 4.1: Parameters value for 22nm technology node

Parameters	**Low-k dielectric (SiO_2)**	**High-k dielectric (HfO_2)**
I_{on}	1.615e-05	6.14e-05
I_{off}	3.207e-15	5.821e-16
DIBL (mV/V)	40.35	13.56
SS (mV/decade)	66.01	60.76

Table 4.2: Parameters value for 14nm technology node

Parameters	Low-k dielectric (SiO_2)	High-k dielectric (HfO_2)
I_{on}	4.18e-05	7.749e-05
I_{off}	1.938e-14	5.261e-15
DIBL (mV/V)	41.92	14.93
SS (mV/decade)	68.99	62.31

From the above table 4.1 and 4.2 it is observed that the best value of drive current, leakage current, DIBL and SS has been obtained for high-k dielectric material for both technology node.

Summary and Conclusions

Chapter 5 SUMMARY AND CONCLUSION

This thesis "Performance evaluation of 22nm and 14nm TG-FinFET using parametric analysis" is a study of FinFET at 22nm & 14nm technology nodes. Since the technology scaling below 45nm has brought several detrimental effects such as increased leakage current and short channel effects, hence, to face all the formidable challenges in the nanometer regime, FinFET has emerged as the best successor device.

For this study, Tri-gate FinFET (TG-FinFET) structure of 22nm and 14nm device has been designed by using the structure given by hisamoto *et al*. on Visual TCAD tool. The process parameters such as fin height, fin width, channel doping, oxide thickness and underlap length has been included for the study in both low-k dielectric material and high-k dielectric material and the device performance has been observed. The simulated results of various parameters of FinFET such as Drive current, Leakage current and DIBL are evaluated that have considerable impact on the performance of the device.

From the simulation it has been observed that in 22nm Technology node the value of drive current obtained is approximately 3.57e-0.5 and 9.80e-05 for low-k and high-k dielectric material respectively, leakage current obtained for low-k & high-k dielectric material is 9.87e-12 and 4.82e-15 respectively. The values of SS (mV/decade) were 70.9 and 63.65 and DIBL (mV/V) were 37.18 and 31.03 for low-k dielectric and high-k dielectric material respectively. Similarly, for 14nm technology node the drive current obtained is approximately 7.83e-0.5 and 1.45e-04 for low-k and high-k dielectric material respectively, leakage current for low-k dielectric material for high-k dielectric material is 5.18e-10 and 1.23e-13 respectively. The values obtained for SS (mV/decade) were 78.24 and 72.56 and DIBL (mV/V) values attained were 75.12 and 63.47 for low-k dielectric and high-k dielectric material respectively. Considering all the parameters at which device is giving better performance i.e. height on fin 10nm, width of fin 5nm, doping concentration 1e19, underlap length 10nm and oxide thickness 1.2nm and 0.8nm for 22nm and 14nm respectively. The obtained values for 22nm technology node with low-k dielectric are 1.615e-05, 3.207e-15, 40.35mV/V and 66.01mV/decade for drive current, leakage current, DIBL and SS respectively. For high-k dielectric material at 22nm technology node the values obtained for drive current, leakage current, DIBL and SS are 6.14e-05, 5.821e-16,

13.56mV/V and 60.76mV/decade respectively. Similarly for low-k dielectric material at 14nm technology node the evaluated values for drive current, leakage current, DIBL and SS are 4.18e-05, 1.938e-14, 41.92mV/V and 68.99mV/decade respectively. For high-k dielectric material at 14nm technology node the values obtained for drive current, leakage current, DIBL and SS are 7.749e-05, 5.261e-15, 14.93mV/V and 62.31mV/decade respectively.

Among all the process parameters the best values have been taken for further simulation and hence it is concluded that device with high-k dielectric shows better performance and reduced short channel effects than the low-k dielectric device. For future work the device may be fabricated and tested for the studied performance.

Literature Cited

LITERATURE CITED

Abraham, N., Parakh, A., C., Unni (2017). Modeling and Simulation Studies of 22nm Multigate bulk FinFET Structures with Different Dielectric Materials. *International Journal of Electronics Engineering Research,* Vol. 9, No. 2, pp. 255-266

Bhattacharya, D., Jha, N.K. (2014). FinFETs: From Devices to Architectures. *Hindawi Active and Passive Electronic Components*

Bukkawar, S., Sarwade, N. (2012). Low leakage nanoscaled source and drain over insulator finfet with underlap and high k dielectric. *International Journal of Engineering Science and Technology (IJEST),* Vol. 4, No. 5, pp. 2300-2306

Chan, T.Y., Chen, J., Ko, P.K., Hu, C. (1987). The Impact of Gate-Induced Drain Leakage Current on MOSFET Scaling. *International Electron Devices Meeting,* Vol. 31, No. 3, pp 718-721, pp. 718-721

Chauhan, Y. S., Duarte, J. P., Gu J. J., Hu C., Khandelwal S., Paydavosi N., Si M., Ye P. D. (2015). FinFET modeling using industry standard compact model BSIM-CMG., *Elsevier press,* pp 1-10

Fasarakis N., Tsormpatzoglou, A., Tassis, D. H., Pappas, I., Papathanasiou, K., Bucher, M., Ghibaudo, G., Dimitriadis, C. A. (2012). Compact Model of Drain Current in Short-Channel Triple-Gate FinFETs. *IEEE transactions on electron devices,* Vol. 59, No. 7, pp. 1891-1898

Frank, D. J., Dennard, R.H., Nowak, E., Solomon, P.M., Taur, Y., Wong, H. N. P. (2001). Device Scaling Limits of Si MOSFETs and Their Application Dependencies. *Proceedings of The IEEE,* Vol. 89, No. 3, pp. 259-288

Godoy, A., Villanueva, J.A.L., Tejada, J.A.J., Palma, A., Gamiz, F. (2001). A simple subthreshold swing model for short channel MOSFETs. *Solid state electronics, Elsevier,* pp. 391-397

Gonzalez, R., Gordon, B.M., Horowitz, M.A. (1997). Supply and Threshold voltage scaling for low power CMOS. *IEEE Journal of Solid State Circuits,* Vol. 32, No. 8, pp. 1210-1215

Hajare, R., Lakshminarayana, C., C. S., Sumanth, R, A. A. (2015). Design and evaluation of FinFET based digital circuits for high speed ICs. *International Conference on Emerging Research in Electronics, Computer Science and Technology,* pp. 162-167

Havaldar, D. S., Katti, G., Gupta, N. D., Gupta, A. D. (2006). Subthreshold Current Model of FinFETs Based on Analytical Solution of 3-D Poisson's Equation. *IEEE Transactions on Electron Devices,* Vol. 53, No. 4, pp. 737-742

Hisamoto, D., Lee, W.C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C., Anderson, E., King, T. J., Bokor, J., Hu, C. (2000). FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm. *IEEE Transactions on Electron Devices,* Vol. 47, No. 12, pp. 2320-2325

Hossain, M. Z., Hossain, M. A., Islam, M. S., Rahman, M. M., Chowdhury, M. H. (2011). Electrical Characteristics Of Trigate FinFET. *Global Journal of Researches in Engineering,* Vol. 11, No. 7

Kaur, N., Rattan, M., Gill, S. S. (2016). Impact of Gate Oxide Thickness and Aspect Ratio of Fin Height and Fin Width on Nanoscale Tapered FinFETs. *IEEE International Conference On Recent Trends In Electronics Information Communication Technology*

Kedzierski, J., Ieong, M., Nowak, E., Kanarsky, T. S., Zhang, Y., Roy, R., Boyd, D., Fried, D., Wong, H. S. P. (2003). Extension and Source/Drain Design for High-Performance FinFET Devices. *IEEE Transactions on Electron Devices,* Vol. 50, No. 4, pp. 952-958

Kloes, A., Weidemann, M., Schwarz, M. (2010). Analytical current equation for short channel SOI multigate FETs including 3D effects. *Solid-State Electronics, Elsevier,* pp. 1408-1415

Mishra, K., Somra, N., Sawhney, R. S. (2015). Simulation of n-FinFET Performance Reliance on Varying Combinations of Gate Material and Oxide. *Communications on Applied Electronics (CAE),* Vol. 2, No. 7, pp. 12-16

Mittal, S. (2016). A survey of architectural techniques for managing process variation. *ACM Computing Surveys (CSUR),* Vol. *48,* No.*1*, pp 1-29.

Moore, G.E. (1998). Cramming More Components onto Integrated Circuits. *Proceedings of IEEE,* Vol. 86, No. 1, pp 82-85

Park, J.T., Colinge, J.P. (2002). Multiple-Gate SOI MOSFETs: Device Design Guidelines. *IEEE transactions on electron devices,* Vol. 49, No. 12, pp. 2222-2229

Revathy, G., Rajak, A. (2014). A survey on finfets: technology, pros, cons and improvement prospects. *International Journal of Advanced Technology in Engineering and Science.* Vol. 2 No. 10, pp. 229-237

Roy, K., Mukhopadhyay, S., Meimand, H.M. (2003). Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits. *Proceedings of the IEEE,* Vol. 91, No. 2, pp. 305-327

Sachid, A.B., Manoj, C.R., Sharma, D. K., Rao, V.R. (2008). Gate Fringe-Induced Barrier Lowering in Underlap FinFET Structures and Its Optimization. *IEEE Electron Device Letters.* Vol. 29, No. 1, pp. 128-130

Saini, G., Rana, A. K. (2011). Physical Scaling Limits of FinFET Structure: A Simulation Study. *International Journal of VLSI design & Communication Systems (VLSICS).* Vol. 2, No. 1, pp. 26-35

Saini, G., Rana, A. K., Pal, P. K., Jadav, S. (2010). Leakage behavior of underlap FinFET Structure: A simulation study. *International conference on Computer & Communication Technology (ICCCT),* pp. 302-305

Saremi, M., Kusha, A. A., Mohammadi, S. (2012). Ground plane fin-shaped field effect transistor (GP-FinFET): A FinFET for low leakage power circuits. *Microelectronic Engineering, Elsevier,* pp. 74-82

Sedra, A. S., Sedra, D. E. A. S., Smith, K. C., & Smith, K. C. (1998). *Microelectronic circuits*. New York: Oxford University Press.

Shukla, S., Gill, S. S., Kaur, N., Jatana, H. S., Nehru, V. (2017). Comparative Simulation Analysis of Process Parameter Variations in 20nm Triangular FinFET. *Hindawi Active and Passive Electronic Components*

Singh, D., Pradhan, K. P., Mohapatra, S.K., Sahu, P.K. (2015). Optimization of Underlap Length for DGMOSFET and FinFET. *International Conference on Recent Trends in Computing, Elsevier,* pp. 448-453

Soman, S., Nirmal, D., Nair, P. P., Ramya, M. S. A., Jeba, K. (2013). Analysis of Drain Current in Short Channel Drain- Extended Triple Gate FinFETs. *Proceedings of the IEEE,* pp. 494-497

Sonone, S., Bhatnagar, S.A. (2017). Comparatively Analysis of Various CMOS FINFET Structure. *International Journal of Technology Research and Management,* Vol. 4, pp. 1-5

Tripathi, S. L., Mishra, R., Narendra, V., Mishra, R. A. (2012). Optimization of Pie-gate Bulk FinFET Structure. *International Journal of Computer Applications.* Vol. 59, No. 2, pp. 34-39

Verma, S., Tripathi, S. L. (2020). Process variation and analysis of FinFET for low-power applications. *IOP Conf. Series: Materials Science and Engineering*

Verma, S., Tripathi, S. L., Bassi, M. (2019). Performance analysis of FinFET device using qualitative approach for low-power applications. *Device for Integrated Circuit (DevIC),* pp. 84-88

Veshala, M., Jatooth, R., Reddy, K. R. (2013). Reduction of Short-Channel Effects in FinFET. *International Journal of Engineering and Innovative Technology (IJEIT).* Vol. 2, No. 9, pp. 118-124

Wann, C.H., Noda, K., Tanaka, T., Yoshida, M., Hu, C. (1996). A comparative study of advanced MOSFET concepts. *IEEE Transactions on Electron Devices,* Vol. 43, No. 10, pp. 1742-1753

Woo, D. S., Lee, J.H., Choi, W. Y., Choi, B. Y., Choi, Y. J., Lee, J. D., Park, B. G. (2002). Electrical Characteristics of FinFET with Vertically Nonuniform Source/Drain Doping Profile. *IEEE Transactions on Nanotechnology,* Vol. 1, No. 4, pp. 233-237

Wu, W., LI, X., Gildenblat, G., Workman, G., Veeraraghavan, S., McAndrew, C., Langevelde, R. V., Smit, G. D. J., Klaassen, D. B. M., Watts, J. (2007). PSP-SOI: A Surface Potential Based Compact Model of Partially Depleted SOI MOSFETs. *IEEE, Custom Intergrated Circuits Conference (CICC),* pp. 41-48

Yang, W., Yu, Z., Tian, L. (2007). Scaling Theory for FinFETs Based on 3-D Effects Investigation. *IEEE Transactions on Electron Devices,* Vol. 54, No. 5, pp. 1140-1146

Appendices

A.1 Review of CMOS

In 1960, at Bell labs Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was introduced by **Shockley *et al.,*** before this in 1930 **Lilienfeld** first patented the concept of Field effect transistor (FET)**.** The device MOSFET has four terminals namely Source (S), Drain (D), Gate (G), Body (B). It is used in switching applications in Digital Circuits, and in amplification activities in Analog Circuits. In MOSFET, when the Body terminal is connected to the Source terminal it forms electronic switch of three-terminals. The insulated gate of MOSFET controls the conductivity by varying the applied potential across the Gate (G) terminal whereas Source (S) terminal remains grounded. A channel is form between Source (S) and Drain (D) regions when the voltage crosses above the threshold voltage level. This would cause the electrons to flow from Source (S) to Drain (D) terminal resulting into Drain (D) current from terminals Drain (D) to Source (S). To revolutionize the ICs the fabrication of NMOS and PMOS transistors on the single wafer is required. When CMOS device is fabricated it shows the advantages of using a single wafer for both NMOS and PMOS transistors. The basic schematic of CMOS is shown in figure 1. The CMOS circuit offer high integration density, very low static power dissipation and high switching speed. The following advantages supports the scaling of MOSFET and with increase in speed, high density ICs are subsequently realized.

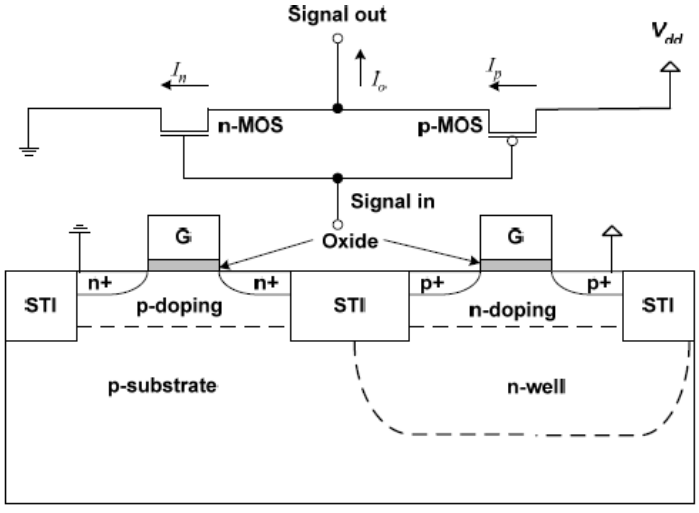


Fig.1: Basic structure of CMOS

A.2 Scaling in the CMOS Technology

The process of reducing the dimensions or the size of a MOSFET is known as Scaling. The first comprehensive guidelines of scaling was "constant field scaling" theory that was given by **Dennard *et al*. (1974)** which states that, to boost the performance of a transistor, its dimensions and power supply should be reduced linearly whereas doping concentration should go up in such a manner that the electric field remains at a constant value in the device.

The dimensions of a MOS are channel length, channel width and oxide thickness. Since the design of high density integrated chips in Very large scale integration (VLSI) technology needs the packing density of MOSFET used in the circuit is as high as possible and the size of transistors are as low as possible. Decreasing the size of all these parameters by a scaling factor S (S<1) will decrease the size of a MOSFET. With the reduction in dimensions of a MOSFET it is expected that the operational characteristics will also get changed and due to some limitations it eventually confine the scaling of a transistor that we can achieve practically. The proportional scaling of devices will result in the reduction of total silicon area that is occupied by the circuit and thereby the functional density of chips gets increased. Basically there are 2 types of size reduction techniques (a) Full Scaling (Constant Field Scaling) (b) Constant voltage Scaling

(a) Full Scaling (Constant Field Scaling)

This technique tries to maintain the internal electric field magnitude of a MOSFET constant as the device dimensions are scaled down by a scaling factor S. The internal potential, power supply and terminal voltage are also scaled down by the scaling factor, which may cause issues as peripheral chips need adequate power supply and so this method is not widely used.

(b) Constant voltage Scaling

This technique is preferred over the constant field scaling since in this the dimensions are reduced but power supply and terminal voltages remain same.

In figure 2, it is shown that the right hand side is new scaled device according to the rule of constant field scaling. In every new generation it's just about double the circuit density and the performance was increased by 40%. According to the ideal scaling rule, as the voltage and the dimension is reduced by the part of √2, switching

delay decreases by an aspect of √2 ,the area density gets doubles and the switching energy is halved.

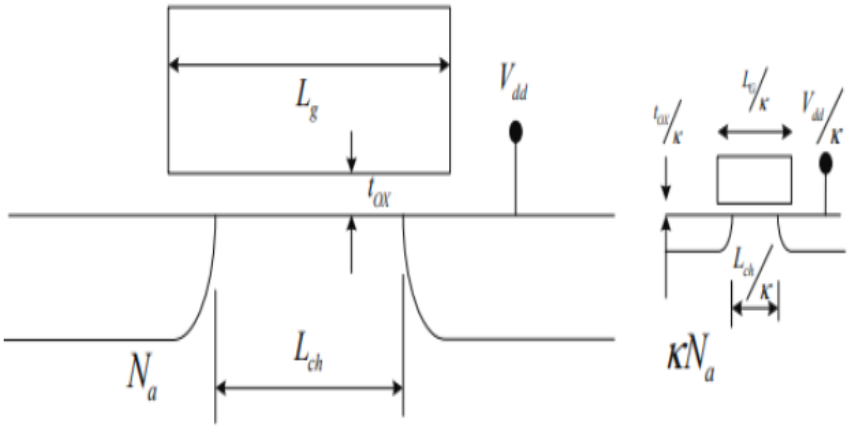


Fig. 2: Miniaturization of MOSFET

Table 1: Scaling rules summary (Dennard *et al.* (1974)

Scaled Parameters	Constant field Scaling	Generalized Scaling
t_{ox}, L, W, X_J, W_d	$1/\kappa$	$1/\kappa$
N_a, N_d $(ions/cm^3)$	κ	$\alpha\ \kappa$
Power supply: (V_{dd})	$1/\kappa$	α/κ
Electric field in device: (E)	1	α
Capacitance: (C)	$1/\kappa$	$1/\kappa$
Inversion charge density (Q)	1	α
Circuit delay time: τ CV/I	$1/\kappa$	$1/\kappa$
Power dissipation: (P)	$1/\kappa^2$	α^2/κ^2
Power density: $(\sim P/A)$	1	α^2
Circuit density	κ^2	κ^2
Chip Area (A)	$1/\kappa^2$	$1/\kappa^2$
Current, Drift: (I)	$1/\kappa$	$1/\kappa$

Table 1 summaries the result of the variation in device dimensions and circuit parameters as the constant field and generalized scaling rules. The scaling factor of *k* is related to 80% reduction in the size of the technology nodes in every two years and the other scaling constant α is used to denote electric field and potential in the generalized scaling scenario.

Advantages of Scaling

1. More chips are created per silicon wafer.
2. If MOSFET becomes smaller they will consume less power as per Dennard scaling law.
3. Smaller transistors switch faster.
4. Packing density of chips increases with the scaling which produces faster and better chips.

Disadvantages of Scaling

1. Smaller MOSFETs have higher leakage current and lower output resistance.
2. Decreasing the oxide thickness can cause it to lose its dielectric property.
3. Smaller MOSFETs have more noise.

A.3 Challenges due to Scaling

In order to follow Moore's law the MOS device has the scaling limit of 22nm beyond this limit MOS device could not be scaled. Beyond 22nm the device not only follows Newton's physics but also follow quantum mechanics. So we need to move to another device to which we can scale below 22nm. As the transistor is scaled down the process complications make it difficult to speculate also additionally any micro changes in the device are probabilistic in nature of atomic process which requires statistic prediction. After combining such factors to make various simulations the following challenges are faced

- **Physical challenge:** When we scale MOS device the tunnelling arises due to which leakage current produces and it affect the performance of the device.
- **Material challenge:** The inability of dielectric and wiring material to provide better isolation to the device and conduction by continued scaling.
- **Heating challenge:** With the scaling of device, as the number of transistors in per unit area gets increased due to which it results in large power consumption and dissipation.
- **Economical challenge:** As the technology is scaled down the fabrication complexity increased due to which cost of production and testing will be increased which is not economical.

A.4 Short channel Effects

To achieve higher packing density, higher performance and low power consumption the scaling of MOS device is done by more than 50 years. The delay in transistor is reduced by 25% as per technology generation as a result of which the speed of microprocessor gets doubled in every 18 months. To maintain the power consumption, power supply voltage is also scaled down. The threshold voltage of device also scaled down to achieve better performance and large drive current. Although the threshold voltage scaling results in increment of sub threshold leakage current. The off state current is influenced by surface or channel doping, gate oxide thickness, threshold voltage, physical dimension of channel, drain/source junction depth and the supply voltage. The short channel transistor needs lower power supply to decrease the internal electric field and power consumption.

A MOSFET device is considered to be short when the length of channel is of same order of depletion layer width of drain and source. As the length of channel becomes shorter, it enters into deep submicron region so various effects came into existences, which are known as short channel effects.

The short channel effects are attributed to 2 physical phenomenons (a) The limitation imposed on electron drift characteristics in the channel (b) The modification of threshold voltage due to the shortening of channel length.

The different short channel effects are follows:

A.4.1 Drain induced barrier lowering

DIBL (Drain induced barrier lowering) is the effect of drain voltage on the output conduction and observe the threshold voltage. This phenomenon is measured as the threshold voltage variation with decreased gate length, which occurs in devices where only gate length is decreased without scaling any other dimensions.

In small–geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage (VGS) and the drain-to-source voltage (VDS). When the drain voltage is increased, the depletion region below the drain increase and it starts contributing with the gate voltage to form the channel results in the decrement of threshold voltage. DIBL occurs mainly due to the contribution of drain electric field over the channel. When the length of channel is long the effect of drain electric field is

less but for short length channel the drain electric field effect increases by lowering the barrier height, which results in further decrement of threshold voltage. The effect of DIBL can be reduced by shallow drain/source junction and by high doping of channel.

A.4.2 Punch Through

In MOSFET punch through is the case of channel length modulation where the depletion region of source and drain merge and form a single depletion region. When the drain voltage increases the depletion region below the drain and well junction also get increased and in this process at a particular voltage the drain and source depletion region interact as a result of this the current starts flowing and since there is no potential barrier it increases drastically. The amount of current flow is so high that it becomes impossible to turn off the device. This undesirable effect increases the output conduction which limits the peak operational voltage of the device. The punch through is of 2 types:

- **Surface punch through:** When the punch through occurs at the surface and current flows through surface is known as surface punch through.
- **Bulk punch through:** When non-uniform doping is done due to ion-implantation. The region under the surface is heavily doped to control the threshold voltage due to this, the depletion starts extending in the bulk and the punch through occurs in the bulk. It is known as bulk punch through.

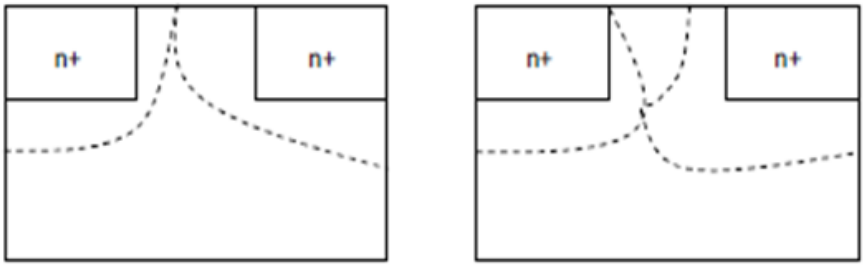


Fig. 3: Surface and Bulk Punch through

A.4.3 Subthreshold leakage

In order to reduce the internal electric field and power consumption, lower power supply is required and hence lower threshold voltage is desired. The Subthreshold leakage or weak inversion current between the source and drain occurs when the gate voltage (Vg) is lower than the threshold voltage (V_{th}).The equation of subthreshold current is

$$I_{ds} = \mu_0 \, c_{ox} \left(\frac{w}{l}\right) * (m-1) * v_t^2 * \left[e^{\left(v_g - v_{th}/mv_t\right)}\right] * \left[1 - e^{\left(-v_{ds}/v_t\right)}\right]$$

Where,

$m=1+C_{dm}/C_{ox} = 1+3t_{ox}/w_{dm}$

μ_0 : Zero bias mobility

c_{ox}: Gate oxide capacitance

m: Subthreshold swing

v_g: Gate voltage

v_t: Thermal voltage

v_{th}: Threshold voltage

$w_{dm:}$ Maximum depletion layer width

A.4.4 Injection of Hot Carriers

In short channel MOSFET, due to the high electric field near silicon oxide (SiO_2) /silicon (Si) interface, the charge carriers are able to gain more energy from higher electric field to cross the surface potential barrier and thus jump into the oxide region. As these high energy electrons enters in the oxide region, there they can be trapped and hence they give rise to oxide charging that can accumulate with time and degrade the device performance by increasing V_t and also affect adversely the gate's control on the drain current. This effect is known as hot carrier injection. This injection is more likely for electrons than holes because electron has smaller effective mass than that of hole and also barrier height of electron is smaller than hole.

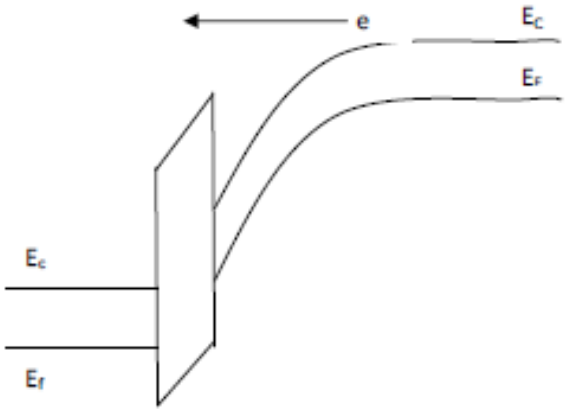


Fig. 4: Injection of hot carrier from substrate to oxide

A.4.5 Velocity Saturation

As we move towards short MOSFET, the performance of short channel devices also gets affected by velocity saturation. The velocity of charge carriers is linearly proportional to the electric field but after certain value of electric field, the velocity does not increase and enters in saturation region. This happens because of the collision of charge carriers and this electric field is called as critical electric field.

The electron velocity is related to the electric field through the mobility: $V=\mu E$

For higher fields the velocity does not increase with electric field, it results in degradation of mobility because of scattering by vertical field. This leads to earlier saturation of current i.e. before V_{GS}-V_{th} and hence it results in reduction of drain current. The velocity saturation reduces the transconductance of short channel MOSFET devices in the saturation region.

A.4.6 Quantum effects

As the size of transistor is scaled down certain quantum effects are introduced in the behaviour of transistor. This effect occurs in the devices that include tunnelling effect. It is defined as the phenomenon when a subatomic particles probability disappears from one side of the potential barrier and appears on the other side without any probability current appearing inside the well. This leads to the leakage of current. If we continue scaling, it will tend to high power dissipation, also across the reverse bias junction, the high electrostatic field causes large amount of current flow across the junction because of tunnelling of electrons from valence band of p region to conduction band of n region. For tunnelling to arise, total voltage drop across the junction needs to be higher than the band gap.

For 90nm technology the thickness of oxide layer is small, which causes tunnelling from channel to gate oxide because electric field value becomes very high at small sizes whereas, in 10 nm technology the charge carriers are no longer restricted to the source well and start tunnelling through the barrier to drain, so the gate voltage has no control over the MOSFET. All this hampers the scaling process.

A.5 Leakage Current in MOSFET

In short channel MOS devices high leakage current is becoming a considerable factor of power dissipation in circuits. In the deep submicron MOS transistor, three major leakage currents are present which are (a) Junction tunnelling current (b)

Subthreshold leakage current (c) Tunnelling gate oxide leakage current, which are shown in Figure . In this section each leakage current component is described.

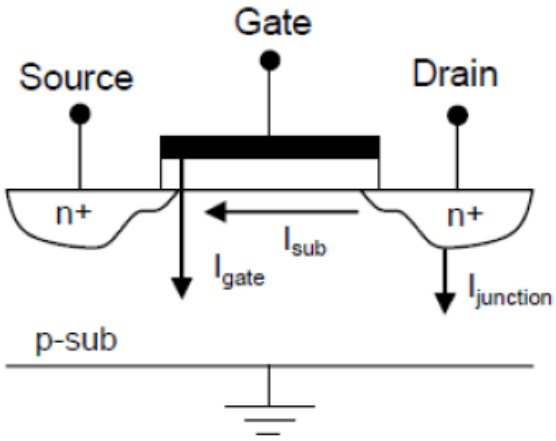


Fig. 5: Leakage current components in a MOSFET

A.5.1 Junction tunnelling current

Within the transistors, a reverse biased junction diode is formed, causing this junction leakage current. This junction leakage occurs from the drain/source region to the substrate region through the reverse biased diodes. When a transistor is in cut off mode. This reversed biased P-N junction leakage has two components: (a) Diffusion of minority charge carriers near the edge of the depletion region and (b) Electron-hole generation pair in depletion region. This leakage current is an exponential function of the reverse biased voltage across the junction and doping. In the present scenario the tunnelling junction leakage current is as small as compared to other leakage currents.

A.5.2 Subthreshold Leakage current

The Subthreshold leakage current occurs in both active mode and standby mode. It is a drain to source current that works at gate voltage which is below the threshold voltage that is in the weak inversion region. The subthreshold region conduction occurs due to the diffusion of minority carriers in the channel of MOS transistor. Standby leakage current occurs when the circuit is idle, where no circuit activity takes place. Therefore, it is recommended to switch off the leakage current when performance is not required, however it is not always possible to shut off the leakage current completely during this period. In general, subthreshold leakage currents are exponentially dependent on temperature, process variations and threshold voltage (V_{th}). The subthreshold leakage current is represented as:

$$I_{SUB} = A_{SUB}\mu_0 C_{OX}\left(\frac{w}{L_{eff}}\right) exp\left(\frac{q}{\eta' kT}(V_{GS} - V_{th} - \gamma' V_{SB} + \eta V_{DS})\right)\left(1 - exp\left(-\frac{q}{kT}V_{DS}\right)\right) \ldots\ldots (A1)$$

Where,

A_{SUB} : (kT/q) 2exp [(1.8)]

V_t : (kT/q) (Thermal voltage)

k : Boltzmann constant

μ_0 : Mobility at zero bias

C_{OX} : Gate oxide capacitance

η' : Subthreshold swing

V_{GS} : Gate to Source voltage

V_{th} : Threshold voltage

γ' : Body effect coefficient

V_{SB} : Source to Bulk voltage

η : DIBL coefficient

V_{DS} : Drain to Source voltage

A.4.3 Tunnelling gate oxide leakage current

In the gate region, electrons or holes tunnelling from the silicon substrate through the gate oxide that results into gate tunnelling current in an NMOS or PMOS. This gate oxide tunnelling current has of three major components:

- Gate to source and gate to drain overlap current.
- Gate to channel current
- Gate to substrate current

In case of planar CMOS, the leakage current between gate -to- body is less than the overlap tunnelling current and gate-to-channel current. The overlap tunnelling current dominates other gate leakage in cut off state, whereas in the ON State due to the tunnelling of gate to channel, gate leakage current increases. The tunnelling gate oxide leakage current is represented as:

$$I_{OX} = A_{OX} W_N L_{eff} \left(\frac{V_{OX}}{T_{OX}}\right)^2 exp\left(-B_{OX} \frac{T_{OX}}{V_{OX}}\right) \quad \text{…. (A2)}$$

Where

A_{OX} and B_{OX} are parameter technologies constant.

V_{OX} is the potential dive across the gate oxide.

VITA

The author, Kanika Tewari was born on 10 November 1995 at Gopeshwar (Uttarakhand). She passed her high school examination in 2010 from SRCBSVMIC Gopeshwar, Chamoli and Intermediate examination in 2012 from SGSVMIC Dehradun. She earned her B.tech degree in Electronics & Communication Engineering from Graphic Era Hill University, Dehradun in year 2016 with first division (honors). She took admission in The College of Post graduate studies in G. B. pant University of Agriculture and Technology in August 2018, for Master's degree in Electronics & Communication Engineering.

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ABSTRACT

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			Degree	:	M.Tech
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Major	:	Electronics and Communication Engineering			
Thesis title	:	**"Performance evaluation of 22nm and 14nm TG-FinFET using parametric analysis"**			
Advisor	:	**Dr. K. K. Sharma**			

Relentless scaling of planar MOSFETs over the past four decades has delivered ever increasing transistor density and performance to the Integrated Circuits (ICs). The continuing trend of scaling of planar MOSFET in nanometer regime has become challenging as it brought several detrimental effects such as increased leakage current and short channel effects (SCEs). Hence, to face these formidable challenges in nanometer regime FinFET has emerged as the best successors.

In this proposed work, a study of various process parameter variations on the operation of Multigate transistor has been done. For this, Tri-gate FinFET (TG-FinFET) structure of 22nm and 14nm device has been designed by using TCAD tool. The parameters such as fin height, fin width, channel doping, oxide thickness and underlap length has been varied for both low-k dielectric material and high-k dielectric material and the device performance has been observed.

The simulation results with high-k dielectric and low-k dielectric were observed. It showed that with the increase in doping concentration and decrease in fin height and width the performance of device improved and the short channel effects reduced. Replacing low-k dielectric with high-k dielectric material results in improvement in device performance.

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सेम और प्रवेश का वर्ष	:	प्रथम, 2018-19	उपाधि	:	एमटेक
			विभाग	:	इलेक्ट्रॉनिक्स और संचार इंजीनियरिंग
प्रमुख विषय	:	इलेक्ट्रॉनिक्स और संचार इंजीनियरिंग			
शोध का शीर्षक	:	"पैरामीट्रिक विश्लेषण का उपयोग करके 22nm और 14nm TG-FinFET का प्रदर्शन मूल्यांकन "			
सलाहकार	:	डॉ0 के.के.शर्मा			

पिछले चार दशकों में प्लानर MOSFETs के लगातार स्केलिंग ने कभी भी ट्रांजिस्टर घनत्व और एकीकृत सर्किट (ICs) के प्रदर्शन को बढ़ाया है। हालाँकि नैनोमीटर शासन में प्लानर MOSFET के स्केलिंग की प्रवृत्ति को जारी रखना चुनौतीपूर्ण हो गया है क्योंकि इसमें कई हानिकारक प्रभाव जैसे रिसाव रिसाव वर्तमान और लघु चैनल प्रभाव (SCE) बढ़ गए हैं। इसलिए नैनोमीटर शासन में इन दुर्जेय चुनौतियों का सामना करने के लिए, FinFET सर्वश्रेष्ठ उत्तराधिकारी के रूप में उभरा है।

इस प्रस्तावित कार्य में, मल्टीग्रेट ट्रांजिस्टर के संचालन पर विभिन्न प्रक्रिया पैरामीटर भिन्नताओं का गहन अध्ययन किया गया है। इसके लिए, 22nm और 14nm डिवाइस के ट्राई-गेट FinFET (TG-FinFET) संरचना को TCAD टूल का उपयोग करके डिजाइन किया गया है। निम्न ऊंचाई, फिन की चौड़ाई, चैनल डोपिंग, ऑक्साइड की मोटाई और अंडरलैप लंबाई जैसे मापदंडों को कम-के-ढांकता हुआ सामग्री और उच्च-के ढांकता हुआ सामग्री दोनों के लिए अलग-अलग किया गया है और डिवाइस के प्रदर्शन को देखा गया है।

सिमुलेशन परिणाम बताते हैं कि डोपिंग एकाग्रता में वृद्धि के साथ डिवाइस का प्रदर्शन बेहतर हो जाता है और लघु चैनल प्रभाव कम हो जाता है। इसके अलावा, उच्च k-ढांकता हुआ का उपयोग करने के प्रभाव को देखा गया है, जिसके परिणामस्वरूप डिवाइस प्रदर्शन में अधिक सुधार हुआ है और कम-k ढांकता हुआ सामग्री की तुलना में लघु चैनल प्रभावों में कमी आई है।

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